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Analysis and design of a soft switched AC-DC converter operating in DCM

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Abstract

This paper presents a soft-switched ac-to-dc boost converter cell operating in discontinuous current mode (DCM). Equivalent circuits for the various operating intervals of the converter are presented and analyzed. Design procedure is illustrated with a design example of a 1 kW, 600 V output ac-to-dc converter cell operating on a 165 to 265 V (rms) utility-line and switching at 100 kHz. Operation and performance of the designed converter is verified using SPICE simulations and experimental results. Detailed loss calculations are given. This converter has low line-current THD and will be used as cells of a multi-phase 5 kW converter.

Keywords: Boost converter, soft-switching, DCM, ZVT, PFC.

1 Introduction

High switching frequency of a power converter is desirable since it results in the small size, light weight, and small input and output current ripple. However, the increased switching loss with the switching frequency is not desirable. The multi-cell converter, with all cells operating in parallel, but each cell at a different phase, is able to achieve similar results in size, weight, and the ripple of the input/output current without suffering the high loss associated with the high switching frequency [1,2], because each cell operates

at a relatively lower frequency than the single-cell converter. The multi-cell configuration has an additional advantage of better thermal control of components. For the above reasons, the phase-shifted multi-cell configuration is adopted for a 5 KW 600 V PFC boost converter, which is the ac-to-dc front stage of an UPS DC power supply. For further reducing the switching losses, without decreasing the switching frequency, the soft-switching technique is applied to each cell. Among various soft-switching circuits [3-17], the ZVT circuit proposed in [3] has the advantages of ease of control, good performance for wide input line voltage and various load conditions. The main switch turns on at zero voltage, whereas the dv/dt of the voltage across the main switch and the di/dt of the current in the boost diode are controlled by the auxiliary circuit. The main switch turns off softly due to the snubber capacitor parallel to it. Therefore its switching losses and the reverse recovery loss of the boost diode can be reduced greatly. The auxiliary switch turns on at zero current, which reduces its turn-on loss.

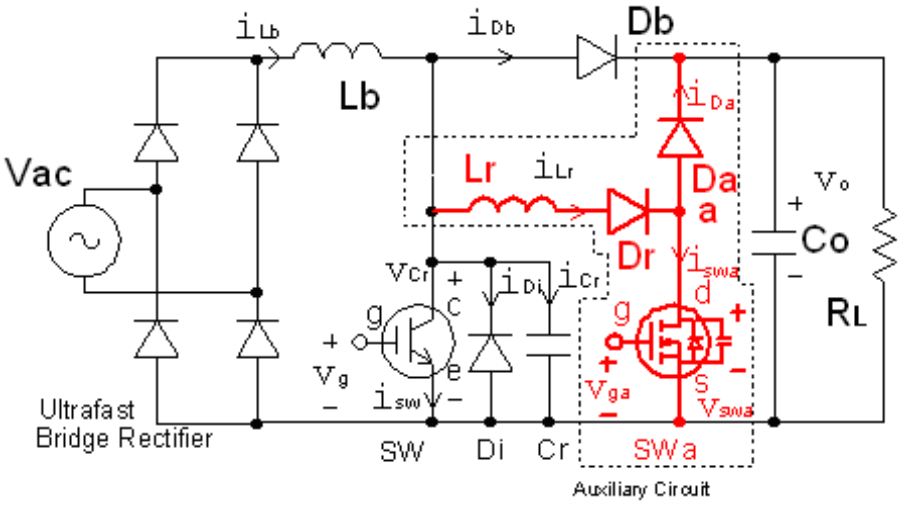


Figure 1: Proposed PFC soft-switched DCM boost converter cell circuit diagram.

While both CCM [2] and DCM [1] operation can be used in the boost converter for a multi-cell configuration, the DCM operation has the following advantages: (1) Power factor correction is achieved using a simple control scheme (natural PFC). (2) The distribution of the power and the input

current is naturally uniform for all cells in the multi-cell system. Unlike CCM operation, it is not necessary for each boost converter cell to sense the inductor current or the switch current. (3) Negligible reverse recovery losses in the boost diode, since the boost diode current slowly returns to zero before the turn-on of the switch in DCM. (4) The ripple cancellation when DCM boost converters operates in multi-phase configuration eliminates the need for large filters.

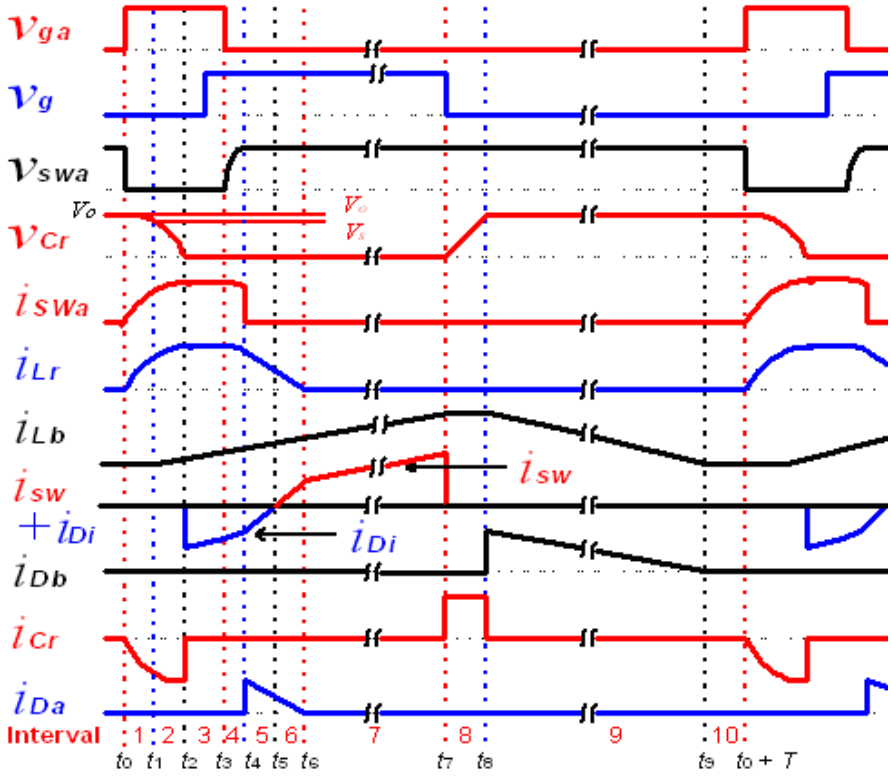


Figure 2: High frequency operating waveforms of the proposed soft-switched DCM boost converter.

Therefore, this paper proposes a soft-switched DCM boost converter cell. Although the proposed cell configuration (Fig. 1) is analyzed for CCM operation [3], its operation, analysis, design, loss calculations, and simulation results for DCM operation are not available in the literature. The layout of the paper is as follows: Section 2 presents the basic operating principle and various intervals of operation. Time domain analyses for the various

intervals are also given. Section 3 gives the design method and loss calculations of the converter based on the above analysis. A 1 kW, 600 V output, 100 kHz, ac-to-dc PFC boost converter cell design example is presented to illustrate the design procedure. Performance of the converter is verified by PSPICE simulation and experimental results presented in Sections 4 and 5, respectively.

2 Operation and analysis of the proposed converter

The operating waveforms are shown in Fig. 2. The equivalent circuits during different intervals for one high frequency (HF) switching cycle are shown in Fig. 3. To simplify the analysis, all the components are assumed ideal and the output capacitor C_o to be equivalent to a constant voltage source. The input line frequency voltage V_s is considered constant in a switching cycle and D_{in} (in Fig. 3) representing the input diode rectifier. The resonant frequency determined by L_r and C_r is very high compared to the switching frequency, f. Operation of the converter and its analysis during different intervals (Figs. 2 and 3) is presented below.

Initially, the main switch SW and the auxiliary switch SWa are in the off-state. The boost inductor current i_{Lb} and the resonant inductor current i_{Lr} are zero. The snubber capacitor C_r is charged to the output voltage (V_o).

Interval 1 (t_0 - t_1)(Fig. 3a): At t_0, the beginning of this interval, the auxiliary switch SWa is turned on. The main switch SW remains off. In this interval the boost inductor current i_{Lb} is zero. Because the current i_{Db} of the diode Db is zero at t_0 under DCM, no reverse recovery current is produced. The resonant current i_{Lr}, which flows through the inductor L_r, capacitor C_r and the diode D_r, starts increasing and the voltage across the snubber capacitor C_r (v_{Cr}) decreasing. The state variables are i_{Lr} and v_{Cr}.

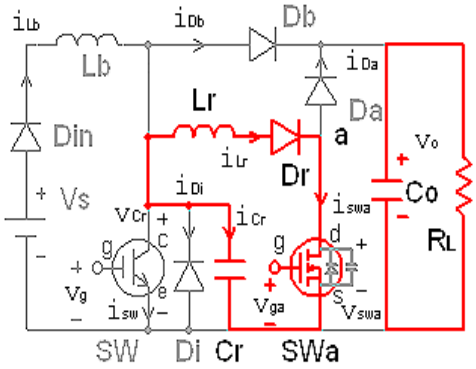
$$i_{Lr} = V_o \cdot \sqrt{C_r/L_r} \cdot \sin[\omega_r \cdot (t - t_0)] \tag{1}$$

$$v_{Cr} = V_o \cdot \cos[\omega_r \cdot (t - t_0)]. \tag{2}$$

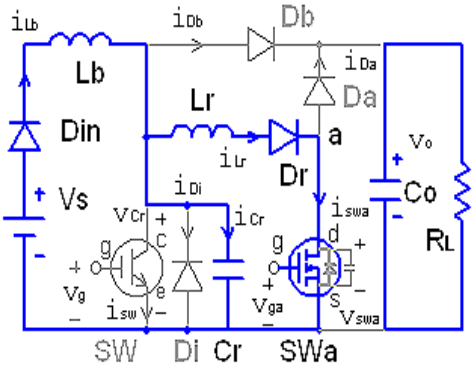
At the end of this interval $(t = t_1), v_{Cr} = V_s$. Therefore,

$$t_1 - t_0 = [\cos^{-1}(V_s/V_o)]/\omega_r \tag{3}$$

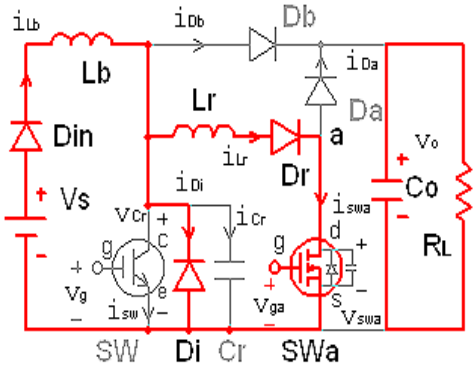
$$\omega_r = 1/\sqrt{L_r \cdot C_r}. \tag{4}$$



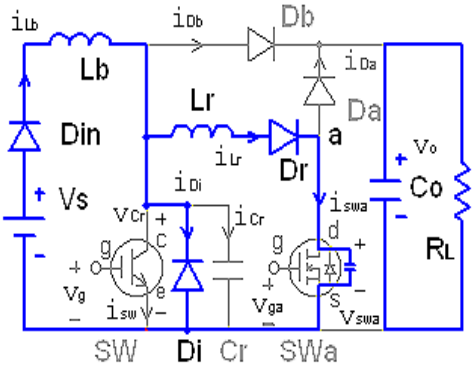
a. Interval 1 (t_0 - t_1)



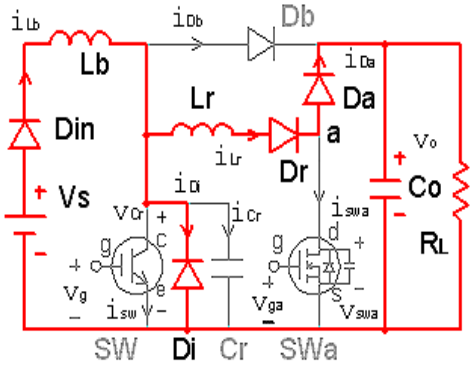
b. Interval 2 (t_1 - t_2)



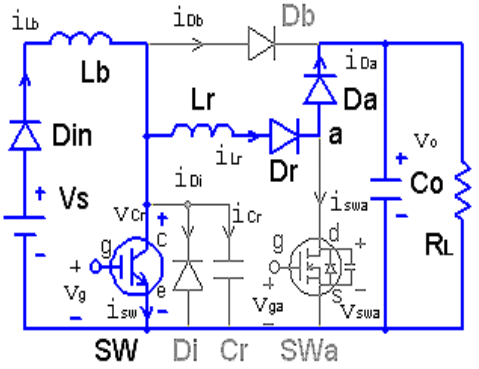
c. Interval 3 (t_2 - t_3)



d. Interval 4 (t_3 - t_4)



e. Interval 5 (t_4 - t_5)



f. Interval 6 (t_5 - t_6)

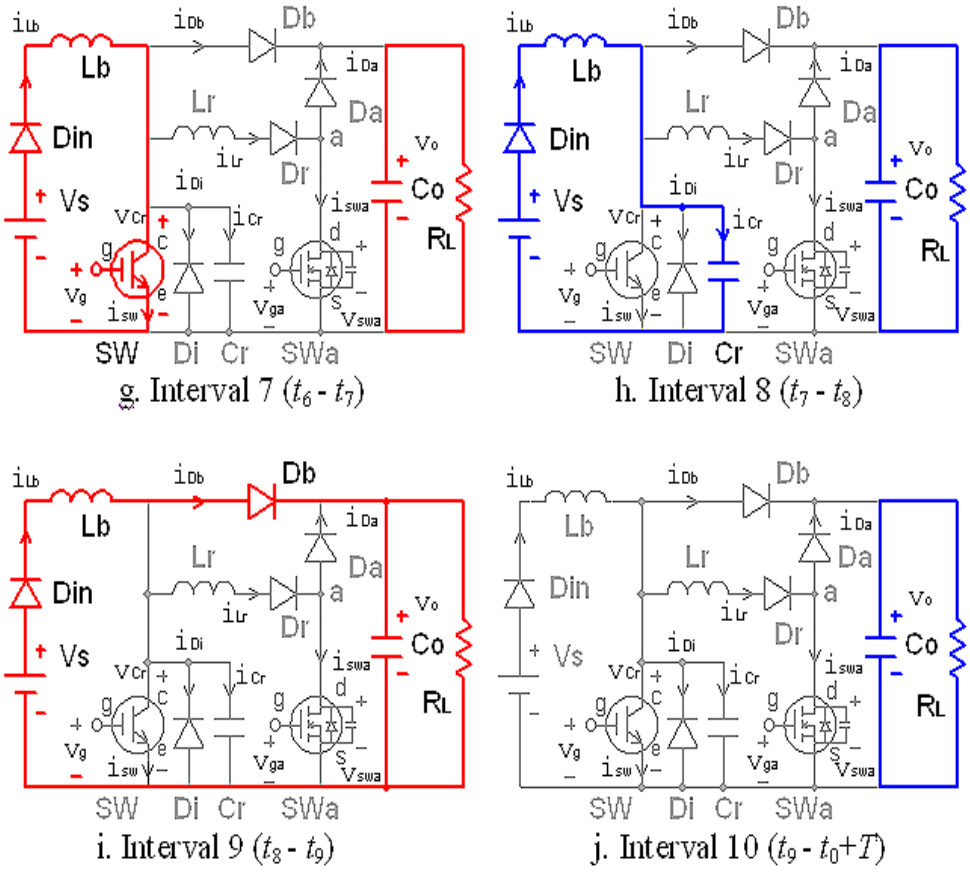


Figure 3: Equivalent circuits of the PFC soft-switched DCM boost converter in different intervals of operation during a HF cycle.

Interval 2 (t_1 - t_2) (Fig. 3b): At $t = t_1$, v_{Cr} decreases to V_s and D_{in} starts conducting. The current in the boost inductor L_b starts increasing from zero. In this interval, the boost inductor current i_{Lb} is very small compared to the resonant inductor current i_{Lr}. Therefore, (1) and (2) approximately describe the current i_{Lr} and the voltage v_{Cr} in this interval, respectively. With the initial condition $i_{Lb}(t_1) = 0$ and v_{Cr} approximated by (2), solution for the boost inductor current i_{Lb} is:

$$\begin{aligned} i_{Lb} \approx\ & V_s \cdot (t - t_1)/L_b - [V_o/(\omega_r \cdot L_b)] \cdot \sin[\omega_r \cdot (t - t_0)] \\ & + [V_o/(\omega_r \cdot L_b)] \cdot \sin[\omega_r \cdot (t_1 - t_0)]. \end{aligned} \tag{5}$$

At the end of this interval, $v_{Cr}(t_2) = 0$, then using (2),

$$t_2 - t_0 = (\pi/2) \cdot \sqrt{L_r \cdot C_r}. \tag{6}$$

The resonant inductor current reaches its maximum value at $t = t_2$, from (1):

$$i_{Lr} = i_{Lr}(t_2) = V_o \cdot \sqrt{C_r/L_r}. \tag{7}$$

From (5),

$$\begin{aligned} i_{Lb}(t_2) \quad \approx \quad & V_s \cdot (t_2 - t_1)/L_b - [V_o/(\omega_r \cdot L_b)] \cdot \sin[\omega_r \cdot (t_2 - t_0)] \\ & + [V_o/(\omega_r \cdot L_b)] \cdot \sin[\omega_r \cdot (t_1 - t_0)]. \end{aligned} \tag{8}$$

Interval 3 (t_2 - t_3) (Fig. 3c): After the voltage v_{Cr} reaches zero, the diode D_i starts to conduct. Then the gate control signal of the main switch SW can be applied. The current i_{Lr} of the inductor L_r is constant in this interval, i.e. $i_{Lr} = i_{Lr}(t_2)$.

The boost inductor current i_{Lb} satisfies

$$i_{Lb} = V_s \cdot (t - t_2)/L_b + i_{Lb}(t_2). \tag{9}$$

The current in diode D_i is

$$i_{Di} = i_{Lb} - i_{Lr}. \tag{10}$$

Interval 4 (t_3- t_4) (Fig. 3d): At $t = t_3$, the auxiliary switch SW_a is turned off. The equivalent output capacitance C_{swa} of the switch SW_a is charged through the diodes D_i and D_r. The current i_{Lb} of the boost inductor L_b continues to increase and is given by (9). With the initial conditions $i_{Lr}(t_3) = V_o(C_r/L_r)^{1/2}$ and v_{swa} $(t_3) = 0$, the resonant inductor current i_{Lr} is

$$i_{Lr} = V_o \cdot \sqrt{C_r/L_r} \cdot \cos[\omega_a \cdot (t - t_3)]. \tag{11}$$

where $\omega_a = 1/(L_r C_{swa})^{1/2}, C_{swa}$ is the switch capacitance of SWa. The voltage across the auxiliary switch

$$v_{swa} = V_o \cdot \sqrt{C_r/C_{swa}} \cdot \sin[\omega_a \cdot (t - t_3)]. \tag{12}$$

The current in diode D_i is given by (10). At the end of this interval v_{swa} $(t_4) = V_o$, thus from (12)

$$t_4 - t_3 = (1/\omega_a) \cdot \sin^{-1}\left(\sqrt{(C_{swa}/C_r)}\right). \tag{13}$$

From (11)

$$i_{Lr}(t_4) = V_o \cdot \sqrt{(C_r \,/\, L_r)} \cdot \cos[\omega_a \cdot (t_4 - t_3)] \tag{14}$$

and from (9)

$$i_{Lb}(t_4) = (V_s/L_b)(t_4 - t_2) + i_{Lb}(t_2). \tag{15}$$

Interval 5 (t_4 - t_5) (Fig. 3e): When the voltage across SW_a reaches the output voltage V_o at $t = t_4$, the diode D_a conducts. v_{swa} is clamped to V_o while diode D_i is still conducting. The boost inductor current i_{Lb} is given by (9). The resonant inductor current is

$$i_{Lr} = i_{Lr}(t_4) - (V_o/L_r)(t - t_4). \tag{16}$$

The current in D_a is the same as i_{Lr} and the current in D_i is given by (10). At the end of this interval $i_{Di}(t_5) = 0$.

Interval 6 (t_5 - t_6) (Fig. 3f): At $t = t_5$, the diode D_i turns off. The main switch turns on with ZVS. The switch current i_{sw} increases while the current i_{Lr} continues to decrease. The main switch currrent is

$$i_{sw} = i_{Lb} - i_{Lr} \tag{17}$$

where i_{Lr} is given by (16). The current in the diode D_a is the same as i_{Lr}. The boost inductor current i_{Lb} is given by (9).

At the end of interval 6, $i_{Lr}(t_6) = 0$. With (16), (14), (13) and $\sin^{-1}[C_{swa}/C_r]^{1/2} \cong 0$.

$$t_6 - t_3 \approx t_6 - t_4 \approx \sqrt{L_r \cdot C_r} \tag{18}$$

$$i_{sw}(t_6) = i_{Lb}(t_6) = (V_s/L_b)(t_6 - t_2) + i_{Lb}(t_2). \tag{19}$$

Interval 7 (t_6 - t_7) (Fig. 3g): In this interval, the circuit operates in the same way as the conventional boost converter. The boost inductor current is given by (9). At the end of this interval, the boost inductor current

$$i_{Lb}(t_7) = (V_s/L_b)(t_7 - t_2) + i_{Lb}(t_2). \tag{20}$$

Interval 8 (t_7 - t_8) (Fig. 3h): At $t = t_7$, the main switch is turned off. In this interval, the boost inductor current is assumed constant, i.e. $i_{Lb} = i_{Lb}(t_7)$. Therefore, the snubber capacitor C_r is charged with the constant current $i_{Lb}(t_7)$. The voltage across snubber capacitor is

$$v_{Cr} = [i_{Lb}(t_7)/C_r](t - t_7). \tag{21}$$

At the end of this interval, v_{Cr} charges to the output voltage V_o ($v_{Cr}(t_7) = V_o$). Thus

$$t_8 - t_7 = [C_r V_o]/i_{Lb}(t_7). \tag{22}$$

Interval 9 (t_8 - t_9) (Fig. 3i): After v_{Cr} is charged to V_o, the boost diode D_b conducts with ZVS. The circuit operates again like the conventional boost converter. The boost inductor current i_{Lb} can be derived from the equation

$$i_{Lb} = i_{Lb}(t_7) - [(V_o - V_s)/L_b](t - t_7). \tag{23}$$

At the end of this interval, $i_{Lb} = 0$ and the diode D_b turns off at zero current.

Interval 10 (t_9 - t_0+ T) (Fig. 3j): This is the DCM interval. i_{Lb} remains zero. The voltage v_{Cr} across the snubber capacitor C_r stays at V_o due to the equivalent blocking diode D_{in}.

3 Design and loss calculations

3.1 Design of the DCM conventional boost converter

This part of design is developed from the analysis given in [18] and [20] for the DCM boost converter operating with a fixed duty cycle and fixed switching frequency. It can be shown that the input power is given by [18,20],

$$P_{in} = [(TV_o^2)/(2\pi \cdot L_b)][D^2 \cdot \alpha^2 \cdot y(\alpha)] \tag{24}$$

where

$$\alpha = 1/M = V_m/V_o, \tag{25}$$

M is the converter gain, DT is the ON-time of the main switch, $D =$ duty ratio of switch SW, $V_o =$ dc output voltage, $V_m =$ peak ac line voltage, $T = 1/f$, $f =$ switching frequency, and

$$y(\alpha) = \frac{-2}{\alpha} - \frac{\pi}{\alpha^2} + \frac{2}{\alpha^2 \cdot \sqrt{1-\alpha^2}} \cdot \left[\frac{\pi}{2} - \tan^{-1}\left(\frac{-\alpha}{\sqrt{1-\alpha^2}}\right)\right]. \quad (26)$$

For the rated power, to ensure the operation in DCM at the peak of line voltage (V_m), the maximum duty ratio, D_m, is

$$D_m = (V_o - V_m)/V_o = 1 - \alpha. \quad (27)$$

Assuming that all the components are ideal, the maximum theoretical value of L_b for DCM operation, denoted by L_{bm}, can be written as (using (24)),

$$L_{bm} = K_b \cdot f_b(\alpha) \quad (28)$$

where

$$K_b = (T \cdot V_o^2)/(2\pi \cdot P_{in}) \quad (29)$$

and

$$f_b(\alpha) = D_m^2 \cdot \alpha^2 \cdot y(\alpha) = (1-\alpha)^2 \cdot \alpha^2 \cdot y(\alpha). \quad (30)$$

In practice, the actual duty ratio D should be less than D_m to ensure DCM operation. This can be assured by selecting the value of $L_b < L_{bm}$, using a duty ratio $D = K_d \cdot D_m$, where $K_d < 1$.

From (28)-(30), it can be seen that L_{bm} is a function of α once the input power P_{in} and output voltage V_o are set by the specifications. We define α as α_L for the minimum input voltage and α_H for the maximum input voltage, respectively. In the design, value of L_b is calculated for these two extreme values. The boost inductance selected is the minimum of the two. Appendix 1 gives the equations used for calculating the component stresses.

3.2 Design of the ZVT circuit

The snubber capacitor limits the dv/dt on the main switch SW and reduces its turn-off loss. The capacitance can be calculated by the equation [20],

$$C_r = I_{SW}(pk) \cdot t_f / V_o \quad (31)$$

where t_f is the fall time of the main switch SW and $I_{SW}(pk) = i_{Lb}(t_7)$ is the peak current (evaluated at the peak of line voltage) of the switch SW.

The selection of the resonant inductance L_r determines the length of the ZVT interval 1 and 2, as well as the peak current of the switch SW_a. From (6) obtained in the analysis of interval 2, L_r can be determined by the equation

$$t_2 - t_0 = K_t \cdot T = (\pi/2) \cdot \sqrt{L_r \cdot C_r} \tag{32}$$

where K_t is the constant assigned to control the length of intervals of the ZVT and T is the HF switching period. Since the resonant frequency of L_r and C_r should be much higher than the switching frequency, K_t can be smaller than 1/20. Thus from (32), the resonant inductance

$$L_r = (1/C_r)(2 \cdot K_t \cdot T/\pi)^2. \tag{33}$$

The peak current of resonant inductor L_r and the auxiliary switch SW_a is

$$I_{Lr}(pk) = I_{SWa}(pk) = i_{Lr}(t_2) = V_o \cdot \sqrt{(C_r \,/\, L_r)}. \tag{34}$$

The average current of diode D_r and inductor L_r is obtained by averaging for the HF cycle for the worst case.

$$\begin{aligned} I_{Dr}(av) &\approx (1/T) \cdot \int_0^{t_6} i_{Lr} dt \qquad (35) \\ &= [V_o.(C_r/L_r)^{1/2}/T][1/\omega_r + (t_3 - t_2) + \sin\{\omega_a \cdot (t_4 - t_3)\}/\omega_a \\ &\quad + (t_6 - t_4) \cdot \cos\{\omega_a(t_4 - t_3)\} - (\omega_r/2) \cdot (t_6 - t_4)^2]. \end{aligned}$$

RMS current of switch SW_a needs to be calculated only over a HF cycle, as the resonant current i_{Lr} repeats in line frequency (LF) cycle in the worst case.

$$\begin{aligned} I_{SWa}(rms) &\approx \sqrt{(1/T)\int_0^{t_4} i_{Lr}^2 dt} \approx \sqrt{(1/T)\int_0^{t_3} i_{Lr}^2 dt} \qquad (36) \\ &= [V_o \cdot (C_r/L_r)^{1/2}][\{\pi/(4\omega_r) + (t_3 - t_2)\}/T]^{1/2}. \end{aligned}$$

Similarly, RMS current of the resonant inductor L_r is obtained also over a HF cycle

$$\begin{aligned} I_{Lr}(rms) &\approx \sqrt{(1/T)\int_0^{t_6} i_{Lr}^2 dt} \qquad (37) \\ &\cong [V_o \cdot (C_r/L_r)^{1/2}][\{\pi/(4\omega_r) + (t_3 - t_2) + (t_6 - t_4) \\ &\quad \times[1 - \omega_r \cdot (t_6 - t_4) + \omega_r^2 \cdot (t_6 - t_4)^2/3]\}/T]^{1/2}. \end{aligned}$$

As C_{swa} is very small compared to C_r, it is assumed that $(t_4 - t_3)$ is zero in the above calculation.

Average current of diode D_a in the worst case

$$\begin{aligned} I_{Da}(av) &\approx (1/T) \cdot \int_{t_4}^{t_6} i_{Lr} dt \\ &= [V_o \cdot (C_r/L_r)^{1/2}/T] \\ &\quad \times [(t_6 - t_4) \cdot \cos\{\omega_a(t_4 - t_3)\} - \omega_r \cdot (t_6 - t_4)^2/2]. \end{aligned} \tag{38}$$

Average current of the diode D_i is obtained by averaging first over the HF cycle and then over the line frequency cycle. Only the worst case is considered. In a HF switching cycle, average current of the diode D_i

$$I_{Di}(av)_s = (1/T) \cdot \int_{t_2}^{t_5} i_{Di} dt. \tag{39}$$

The above integral can be evaluated using the equations for various intervals given in Section 2. Contribution from the boost inductor current before t_2 which is very small, is neglected. Then the average current of D_i in a line cycle ($\omega_l = 2\pi f_l$, f_l = line frequency) is

$$\begin{aligned} I_{Di}(av) &= \frac{1}{\pi} \cdot \int_0^{\pi} I_{Di}(av)_s d(\omega_l t) \\ &= [V_o \cdot (C_r/L_r)^{1/2}/T][(t_3 - t_2) + \sin\{\omega_a \cdot (t_4 - t_3)\}/\omega_a \\ &\quad + (t_5 - t_4) \cdot \cos\{\omega_a(t_4 - t_3)\} - (t_5 - t_4)^2(\omega_r/2)] \\ &\quad - [V_m/(\pi \cdot T \cdot L_b)](t_5 - t_2)^2. \end{aligned} \tag{40}$$

Appendix 2 gives the equations used for the loss calculations.

3.3 Design example

An ac-to-dc boost converter cell with the following specifications is designed to illustrate the design procedure: Input ac voltage, V_{ac}(rms) = 165 - 265 V, 60 Hz. Output power, P_o= 1000 W. Output voltage, V_o = 600 V. Switching frequency, f= 100 kHz.

We assume that the efficiency of the converter is 95% (guess value). Then the input power $P_{in} = P_o/\ 0.95 = 1053$ W.

The values of α for minimum and maximum input voltage are: $\alpha_L = (\sqrt{2}\times 165/600) = 0.3889$ and $\alpha_H = (\sqrt{2}\times 265/600) = 0.6246$, respectively. Then the maximum boost inductance values calculated (using (28)) for DCM

operations for the minimum and maximum input voltages are: $L_{bm} = 72.72$ μH for $V_{ac} = 165$ (r.m.s.) and $L_{bm} = 104.3$ μH for $V_{ac} = 265$ V (r.m.s.). Therefore, the minimum of the two, $L_{bm} = 72.72$ μH for $V_{ac} = 165$ V (r.m.s.) is selected.

From (27), the maximum duty cycle at the minimum ac input voltage $V_{ac} = 165$ V (r.m.s.) is $D_m = 0.611$. To avoid entering CCM, we use 5% margin in setting the limit of the duty cycle, i.e. $K_d = 0.95$. Thus the duty cycle at rated output power, $D = K_d.D_m = 0.5805$. The designed boost inductance, $L_b = K_d^2 L_{bm} = 65.64$ μH.

The component stresses (additional subscripts L and H are used to represent the minimum and maximum input voltage conditions) of the conventional boost converter are as follows:

At the minimum ac input voltage $V_{acL} = 165$ V (r.m.s.), $D = 0.5805$. Using (A1.1 – A1.8) of Appendix 1 with $\alpha = \alpha_L = 0.3889$, $I_{ac}(rms)_L = 6.40$ A, $I_{Lb}(av)_L = 5.57$ A, $I_{SW}(pk)_L = I_{Lb}(pk)_L = 20.64$ A, $I_{SW}(av)_L = 3.81$ A, $I_{Db}(av)_L = 1.67$ A, $I_{BR}(av)_L = 2.78$ A.

At the maximum ac input voltage $V_{acH} = 265$ V (r.m.s.), duty cycle $D = D_H = 0.2978$ (using A1.9) at the rated power. Using (A1.1 – A1.8), in Appendix 1 with $\alpha = \alpha_H$, $I_{ac}(rms)_H = 4.04$ A, $I_{Lb}(av)_H = 3.37$ A, $I_{SW}(pk)_H = I_{Lb}(pk)_H = 17.0$ A, $I_{SW}(av)_H = 1.61$ A, $I_{Db}(av)_H = 1.67$ A, $I_{BR}(av)_H = 1.68$ A.

The warp speed IGBT IRG4PF50WD is selected for the main switch. It has a maximum fall-time of $t_f = 190$ ns. Using (31) and $I_{SW}(pk) = 20.64$ A, we calculate the snubber capacitance $C_r = 6.5$ nF. A bigger standard value $C_r = 8.2$ nF is chosen to reduce the turn-off loss of the main switch SW. We assign $K_t = 1/20$, so that the resonant frequency (f_r) of L_r and C_r is much higher than the switching frequency (f). With (33), calculated resonant inductance $L_r = (1/C_r)(2K_tT/\pi)^2 = 12.3$ μH. We choose $L_r = 12$ μH and MOSFET IRFPF50 for the auxiliary switch. Its fall time is $t_{fa} = 37$ ns.

The output filter capacitance, discussed in [20], is

$$C_o = I_o/(2\omega_l * V_{rp}(pk)). \tag{41}$$

With the peak ripple voltage $V_{rp}(pk) = 5$ V, output current $I_o = 1.67$ A and $\omega_l = 120\pi$ rad/s, calculated $C_o = 442$ μF. We choose $C_o = 470$ μF.

During ZVT intervals, the boost inductor current is small and its effect is neglected in the following calculation. This results in $t_4 - t_3 = 0$, $t_6 - t_5 = 0$ and $t_6 - t_4 \cong \sqrt{L_r \cdot C_r}$. To have enough conduction time of diode D_i to ensure ZVS of the main switch SW, assume that interval 3, $(t_3 - t_2) = 200$ ns. The calculation results are as follows:

Peak current of the resonant inductor L_r and the auxiliary switch SW_a are: $I_{Lr}(pk) = I_{SWa}(pk) = 15.68$ A. $I_{Lr}(rms) = 3.68$ A. Average current of the diode D_r: $I_{Dr}(av) = 1.05$ A. RMS current of auxiliary switch SW_a: $I_{SWa}(rms) = 3.31$ A. Average current of diode D_a: $I_{Da}(av) = 0.25$ A. Average current of the diode D_i: $I_{Di}(av) = 1.05$ A.

The simulation results for the above designed boost converter are given in Section 4.

With C_{swa}= 0.27 nF, t_{fa}= 37 ns, R_{ds}=1.6 Ohm, V_F=1.8 V, $V_{CE}(sat)$ = 1.8 V and $Q = 200$, the calculation results of efficiency are listed in Table 1 for the 1 kW, 600 V output boost converter operating at 100 kHz designed above. In the calculations, it is assumed that, for enough conduction time of the diode D_i to ensure ZVS of the main switch SW, interval 3, $(t_3 - t_2)$ = 200 ns. It is also assumed that $(t_2 - t_0) \approx (\pi/2)\cdot(L_r \cdot C_r)^{1/2} = 492.7$ ns, because i_{Lb} is very small during ZVT intervals.

A converter with the same specifications, except for the output voltage changed to 450 V, was also designed [20]. In this case, L_b has to be selected for the maximum input voltage at rated power (since lower value occurs for this condition) to avoid CCM operation at the minimum input voltage of V_{ac} = 165 V (rms) and full load.

Line Voltage	Load	P_{cond} [W]	P_{coff} [W]	P_{Di} [W]	P_{cond} [W]	P_{Da} [W]	P_{Di} [W]	P_{off} [W]	P_{con} [W]	P_{Db} [W]	P_{BR} [W]	P_{Lb} [W]	SUM [W]	Effi-ciency
165 V (r.m.s.)	100%	4.86	5.80	1.89	17.57	0.44	0.80	3.90	6.86	3.01	20.05	8.45	73.63	93.1%
	50%							1.95	3.43	1.50	10.02	2.11	50.37	90.9%
	25%							0.98	1.72	0.75	5.01	0.53	40.35	86.1%
265 V (r.m.s.)	100%	4.86	5.80	1.89	17.57	0.44	0.68	2.66	2.90	3.01	12.12	3.36	55.29	94.8%
	50%							1.33	1.45	1.50	6.06	0.84	42.42	92.2%
	25%							0.66	0.73	0.75	1.21	0.21	34.80	87.8%

Table 1: Calculation results of losses and efficiency with minimum and maximum line voltage at full load, half load, and 25% load for the 1 kW, 600 V output boost converter operating at 100 kHz designed in Section 3.

4 SPICE simulation results

To reduce the simulation time and the data storage space, the 1 kW, 600 V output boost converter designed in Section 3.3 is re-designed with a switching frequency of 10 kHz. Since the switching frequency is still very high compared to the line frequency, the simulation results will reflect the steady

state analysis, as does the boost converter switching at 100 kHz. The re-design gives the components, obtained by 10 times of the value at 100 kHz, as follows: boost inductanceL_b= 656.4 μH, snubber capacitance C_r= 82 nF, and resonant inductance L_r= 120 μH. The output filter capacitor remains unchanged, C_o = 470 μF.

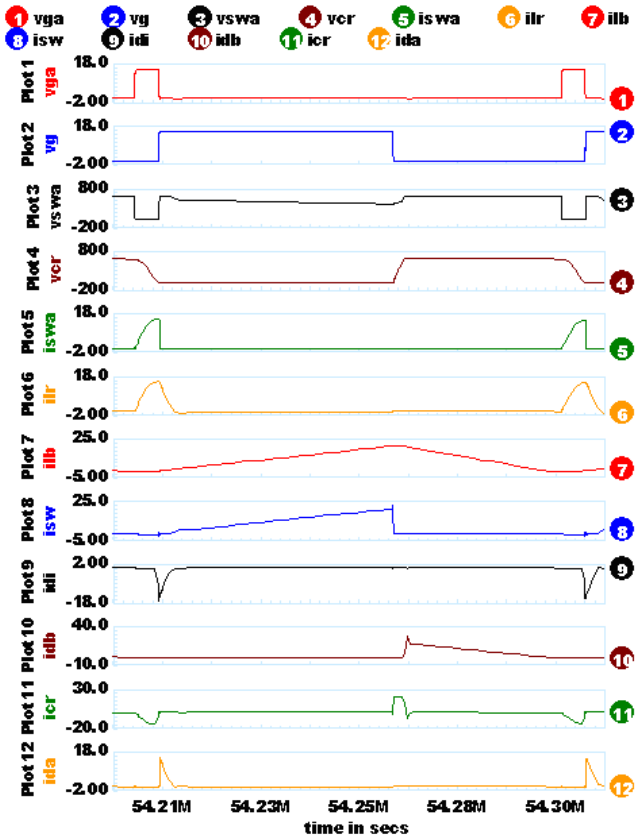


Figure 4: SPICE simulation (on high frequency scale) waveforms obtained with 165 V (r.m.s.) input at full load for the 1 kW, 600 V output converter designed in Section 3.

Typical HF waveforms obtained from the SPICE simulation using INTUSOFT software for the re-designed converter with a minimum input voltage of V_{ac} = 165 V (r.m.s.) at full load and for a maximum input voltage of V_{ac} = 265 V (r.m.s.) at 25% load are shown in Figs. 4 and 5, respectively. These waveforms confirm the HF waveforms of Fig. 2 given in the analysis in Sec-

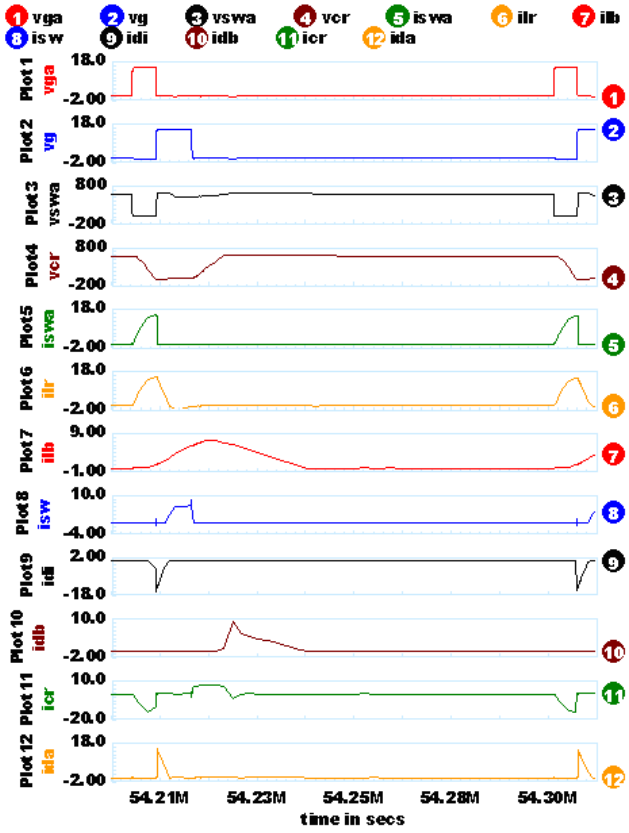


Figure 5: SPICE simulation (on high frequency scale) waveforms obtained with 265 V (r.m.s.) input at 25% load for the 1 kW, 600 V output converter designed in Section 3.

tion 2. In simulation, the interval 3 (t_3–t_2), is very small, reflecting the desired ZVT operation. Since non-ideal diode models are used in the simulation, the waveform of v_{SWa} in the interval 6 is different from that in the analysis, where the ideal diodes are assumed. The reverse recovery characteristic of the diode D_r in series with L_r is the main reason for the difference.

The un-filtered input line-current i_{ac}, line voltage v_{ac} and the harmonic spectra of the high frequency filtered i_{ac} for the conditions given in Figs. 4 and 5 are shown in Figs. 6 and 7, respectively. Table 2 summarizes the component stresses obtained from the SPICE simulation results together

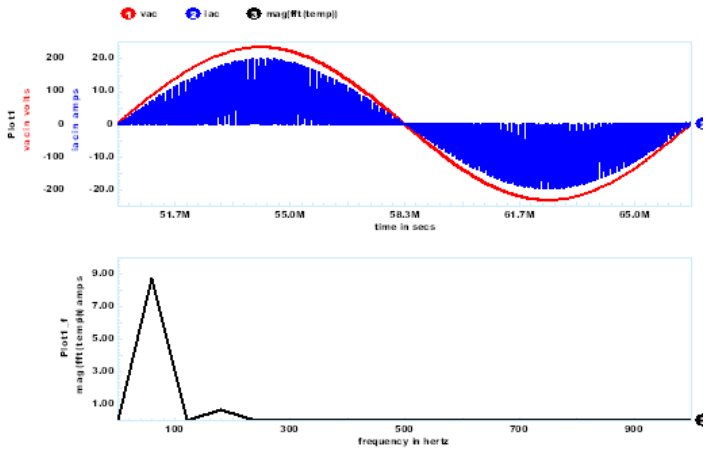


Figure 6: SPICE simulation results: unfiltered input line current iac, line voltage vac and harmonic spectrum of high frequency filtered iac (THD=7.9%) for 1 kW, 600 V output converter with 165 V (r.m.s.) input and at full load.

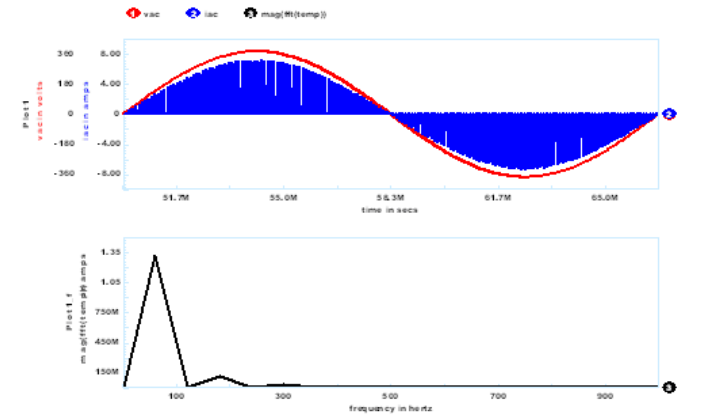


Figure 7: SPICE simulation results: unfiltered input line current iac, line voltage vac and harmonic spectrum of high frequency filtered iac (THD=9.7%) for 1 kW, 600 V output converter with 265 V (r.m.s.) input and at 25% load.

with those obtained from theory. Table 3 summarizes the THD obtained from the SPICE simulation for various input voltages and load conditions.

Line Voltage	Load	Method	$I_{ac}(rms)$ [A]	$I_{Lb}(av)$ [A]	$I_{SW}(pk)$ [A]	$I_{SW}(av)$ [A]	$I_{Db}(av)$ [A]	$I_{BR}(av)$ [A]	D %	$I_{SWa}(pk)$ [A]
165 V (r.m.s.)	100%	Simulation	7.64	5.38	21.98	3.53	1.45	2.69	55	15.49
		Calculation	6.40	5.57	20.64	3.81	1.67	2.78	58	15.68
	50%	Simulation	4.48	2.65	15.64	1.65	0.63	1.33	37	15.38
		Calculation	3.20	2.78	14.59	1.91	0.83	1.39	41	15.68
	25%	Simulation	2.61	1.31	11.04	0.72	0.23	0.66	24	15.37
		Calculation	1.60	1.39	10.32	0.95	0.42	0.70	29	15.68
265 V (r.m.s.)	100%	Simulation	5.43	3.22	17.78	1.36	1.45	1.61	26	15.52
		Calculation	4.04	3.37	17.00	1.61	1.67	1.68	30	15.68
	50%	Simulation	3.19	1.60	12.31	0.56	0.63	0.80	16	15.48
		Calculation	2.02	1.68	12.02	0.81	0.83	0.84	21	15.68
	25%	Simulation	1.86	0.81	8.56	0.19	0.23	0.40	8.6	15.46
		Calculation	1.01	0.84	8.50	0.40	0.42	0.42	15	15.68

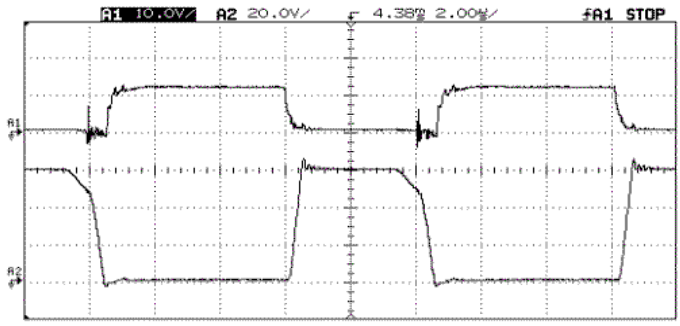
Table 2. Component stresses from simulation and calculation results for the 1 kW, 600 V output boost converter designed in Section 3. Output voltage is regulated at 600 V.

Input	165 V (r.m.s.)			265 V (r.m.s.)		
Load	100% (1 kW)	50%	25%	100% (1 kW)	50%	25%
THD [%]	7.9	6.3	4.1	15.9	13.9	9.7

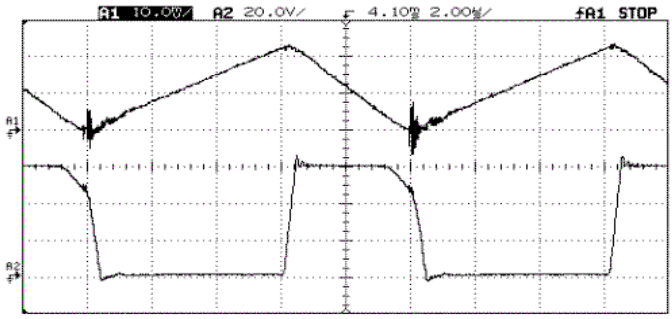
Table 3. THD results of HF-filtered i_{ac} from the simulation for the 1 kW, 600 V output boost converter designed in Section 3.

5 Experimental results

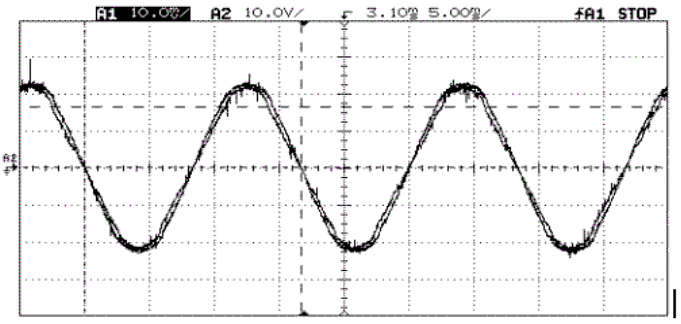
Based on the values obtained in the design example given in Section 3, a 100 kHz, 1 kW, 600 V output ac-to-dc boost converter was built in the laboratory using warp-speed IGBT IRG4PF50WD for the switch SW and MOSFET for the switch SW_a. Fig. 8 shows some sample waveforms obtained with minimum input voltage (165 V r.m.s.) and maximum output power (1 kW) at 600 V output. Fig. 8a shows the soft-switching of the switch SW. Fig. 8b confirms waveforms of i_{Lb} and v_{Cr} predicted in the analysis and obtained in the simulation. Fig. 8c reveals the performance of the power factor



(a) v_g (10 V/div.) and v_{Cr} (200 V/div.)

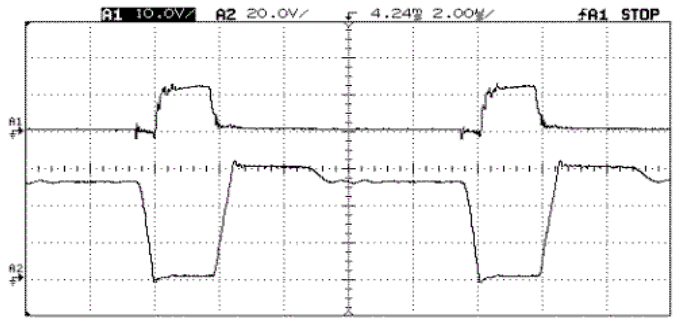


(b) i_{Lb} (10 A/div) and v_{Cr} (200 V/div.)

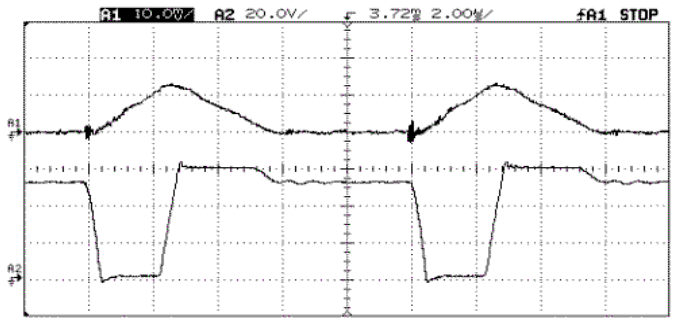


(c) AC line voltage (100 V/div.) and line current (5 A/Div.)

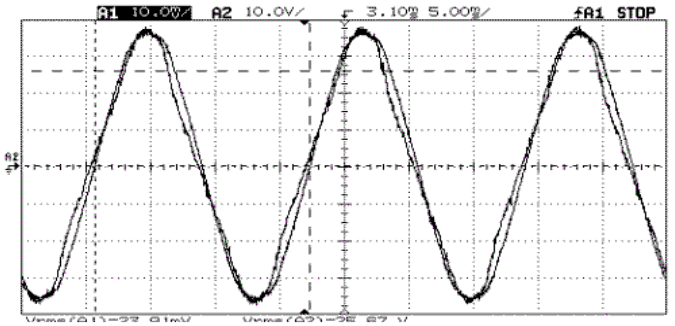
Figure 8: Experimental waveforms obtained for the 1 kW, 600 V output converter with 165 V (r.m.s.) input and at full load.



(a) v_g (10 V/div.) and v_{Cr} (200 V/div.)



(b) i_{Lb} (10 A/div) and v_{Cr} (200 V/div.)



(c) AC line voltage (100 V/div.) and line current (2.5 A/div.)

Figure 9: Experimental waveforms obtained for the 1 kW, 600 V output converter with 265 V (r.m.s.) input and at 50% load.

correction with low THD with the proposed boost converter. Measured efficiency for this condition was about 91.2%, (calculated efficiency is 93.1%). With an input voltage of 265 V (r.m.s.) at half load (500 W) (waveforms shown in Fig. 9), measured efficiency was 92.7%. Measured harmonics amplitudes and THD were very close (with an error of 1% to 2% range) to the simulation results.

6 Conclusions

A soft-switched ac-to-dc converter cell operating in DCM has been proposed. Only one auxiliary switch is used to achieve the soft-switching of the main switch *SW*. The operating intervals and detailed analysis have been presented. The analysis of the operation is confirmed by the simulation results. A design example is given to illustrate the design procedure. SPICE simulation results obtained confirm theoretical results. An experimental 1 kW prototype laboratory model with 600 V output and operating at 100 kHz, is implemented using IGBT for the main switch. Experimental results confirm the theory and show low line-current THD. This converter can be used as a cell for a 5 kW front-end converter. Second stage will be a high frequency transformer isolated dc-to-dc converter to step-down from 600 V to 420 V. The proposed converter is for use in an UPS system. With the availability of fast switching IGBTs and MOSFETs, higher efficiencies can be obtained.

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Appendix 1. Calculation of the component stresses of the conventional PFC boost converter operating in DCM

Main switch peak current

$$I_{sw}(pk) = V_m \cdot D \cdot T/L_b. \tag{A1.1}$$

R.m.s. input current

$$I_{ac}(rms) = I_{Lb}(rms) = P_{in} \cdot \sqrt{\pi} \cdot \sqrt{\beta(\alpha)}/[V_m \cdot y(\alpha)] \tag{A1.2}$$

where

$$\beta(\alpha) = \frac{2}{\alpha \cdot (1-\alpha^2)} + \frac{\pi}{\alpha^2} + \frac{2 \cdot \alpha^2 - 1}{\alpha^2 \cdot (1-\alpha^2)} \cdot \frac{2}{\sqrt{1-\alpha^2}} \cdot \left[\frac{\pi}{2} - \tan^{-1}\left(\frac{-\alpha}{\sqrt{1-\alpha^2}} \right) \right] \tag{A1.3}$$

and $y(\alpha)$ is given by (26).

Other equations for the design are given below. Average switch current

$$I_{sw}(av) = V_m \cdot D^2 \cdot T/(\pi \cdot L_b). \tag{A1.4}$$

Average current of boost diode

$$I_{Db}(av) = P_o/V_o. \tag{A1.5}$$

Average current though each diode in the input bridge rectifier

$$I_{BR}(av) = I_{Lb}(av)/2 \tag{A1.6}$$

where P_o is the output power and $I_{Lb}(av)$ is the average boost inductor current.

$$I_{Lb}(av) = \frac{K1}{\pi} \cdot \int_0^{\pi} \frac{\sin(\omega_l \cdot t)}{1 - \alpha \cdot \sin(\omega_l \cdot t)} d(\omega_l \cdot t) \tag{A1.7}$$

where

$$K1 = P_{in} \cdot \pi/[V_o \cdot \alpha \cdot y(\alpha)]. \tag{A1.8}$$

Its numerical solution can be obtained by using MATHCAD or other math software tools. Once the value of L_b is selected as presented in Section 3, the duty ratio D_p for any other input voltage and P_{in} can be calculated from

$$D_p = [K \cdot P_{in}/\{(\alpha^2 \cdot y(\alpha)\}]^{1/2} \tag{A1.9}$$

where

$$K = (2 \cdot \pi \cdot L_b)/(T \cdot V_o^2). \tag{A1.10}$$

Appendix 2. Loss calculations

Losses in the ZVT circuit are calculated as follows.

Auxiliary switch turn-on loss:

$$P_{ona} = f \cdot C_{swa} \cdot V_o^2/2. \tag{A2.1}$$

Auxiliary switch turn-off loss:

$$P_{offa} = I_{Lr}(pk) \cdot V_o \cdot t_{fa}/(6T) \tag{A2.2}$$

where C_{swa} is the output capacitance of the auxiliary switch and t_{fa} is its fall-time.

For an IGBT, the conduction loss for switch SW_a:

$$P_{cona} = I_{SWa}(av) \cdot V_{CE}(sat). \tag{A2.3}$$

For a MOSFET, conduction loss for switch SW_a:

$$P_{cona} = I_{SWa}(rms)^2 \cdot R_{ds}. \tag{A2.4}$$

Conduction loss for diode D_a:

$$P_{Da} = I_{Da}(av) \cdot V_F. \tag{A2.5}$$

Conduction loss for diode D_r:

$$P_{Dr} = I_{Dr}(av) \cdot V_F. \tag{A2.6}$$

Conduction loss for diode D_i:

$$P_{Di} = I_{Di}(av) \cdot V_F \tag{A2.7}$$

where V_F is the voltage drop of the diodes, R_{ds} is the Drain-to-Source On-Resistance.

Losses in main circuit are calculated as follows.

Main switch SW turn-off loss:

$$P_{off} = V_m^2 \cdot D^2 \cdot T \cdot t_f^2/[48 \cdot L_b^2 \cdot C_r]. \tag{A2.8}$$

Main switch SW (for IGBT) conduction loss:

$$P_{con} = I_{SW}(av) \cdot V_{CE}(sat). \tag{A2.9}$$

Diode D_b conduction loss:

$$P_{Db} = I_{Db}(av) \cdot V_F. \tag{A2.10}$$

Bridge rectifier conduction loss:

$$P_{BR} = I_{Lb}(av) \cdot (2V_F). \tag{A2.11}$$

Boost inductor loss:

$$P_{Lb} = 2 \cdot \pi \cdot f \cdot L_b \cdot [I_{Lb}(rms)]^2/Q. \tag{A2.12}$$

In the above equations V_m is the peak input voltage, D the duty cycle, $V_{CE}(sat)$ the Collector-to-Emitter saturation voltage, $I_{SW}(av)$ the average current of the main switch, $I_{Db}(av)$ the average current of diode D_b, $I_{Lb}(av)$ the average current of boost inductor, $I_{Lb}(rms)$ the rms current and Q the quality factor of L_b. Then the total loss is calculated from

$$P_{Loss} = P_{ona}+P_{offa}+P_{cona}+P_{Da}+P_{Dr}+P_{Di}+P_{off}+P_{con}+P_{Db}+P_{BR}+P_{Lb}. \tag{A2.13}$$

References

[1] B.A. Miwa, D.M. Otten, and M.F. Schlecht, IEEE Applied Power Electronics Conf. (APEC'92), Boston, MA, p.557 (1992).

[2] L. Balogh and R. Redl, IEEE Power Electronic Specialists Conference (PESC'93), Seattle, WA, p.168 (1993).

[3] G. Hua, C. Leu and F.C. Lee, IEEE Trans. on Power Electronics **9**, 213 (1994).

[4] R. Streit and D. Tollik, Proc. 13th Telecommunication Energy Conference INTELEC'91, Kyoto, Japan, p.720 (1991).

[5] H. Bodur and A.F. Bakan, IEEE Trans. on Power Electronics **17**, 40 (2002).

[6] L.C. de Freitas and P.R.C. Gomes, 24th Annual IEEE Power Electronic Specialists Conference (PESC'93), Seattle, WA, p.330 (1993).

[7] M.M. Jovanovic, IEEE Trans. on Power Electronics **13**, 932 (1998).

[8] J.A Bassett, Proc. 17th Telecommunication Energy Conference INTELEC'95, The Hague, Netherlands, p.813 (1995).

[9] K.M. Smith Jr. and K.M. Smedley, IEEE Trans. on Power Electronics **12**, 376 (1997).

[10] G. Moschopoulos, P. Jain, Y.F Liu, and G. Joos, 27th Annual IEEE Power Electronic Specialists Conference (PESC'96), Baveno, Italy, vol.**1**, p.76 (1996).

[11] R. Gurunathan and A.K.S. Bhat, IEEE Power Electronic Specialists Conference (PESC'99), Charleston, SC, USA, p.463 (1999).

[12] H. Mao, F.C.Y. Lee, X. Zhou, H. Dai, M. Cosan, and D. Boroyevich, IEEE Trans. on Ind. Applications **33**, 1220 (1997).

[13] I.D. Jitaru, Proc. High-Frequency Power Conv. Conf., Washington, DC, p.202 (1993).

[14] D.M. Xu, C. Yang, L. Ma, C. Qiau, Z. Qian, and X. He, IEEE Applied Power Electronics Conf. (APEC'97), Atlanta, GA, vol.**1**, p.266 (1997).

[15] C.M. Duarte and I. Barbi, IEEE Trans. on Power Electronics **12**, 824 (1997).

[16] G. Arun, W.S. Shiren, and P.N. Enjeti, IEEE Trans. on Power Electronics **13**, 308 (1998).

[17] G. Hua, E. Yang, and F.C. Lee, IEEE Power Electronic Specialists Conference (PESC'93), Seattle, WA, p.538 (1993).

[18] K.H. Liu and Y.L. Lin, IEEE Power Electronic Specialists Conference (PESC'89), Milwaukee, WI, vol. **2**, p.825 (1989).

[19] P. Chen, *Soft-switched, power factor corrected, discontinuous current mode AC-to-DC boost converters and extension to interleaved converter*, M.A.Sc. Thesis, Dept. of ECE, University of Victoria, BC, Canada, Sept. 2004.

[20] R. Venkatraman, *A soft-switching single-phase single-stage ac-to-dc converter with low line current harmonic distortion*, M.A.Sc. Thesis, Dept. of ECE, University of Victoria, BC, Canada, 1998.