Selection of process parameters for statistical timing

Peter A. Habitz, IBM

Chip static timing has to ensure functionality of the chip under many different conditions. These are different environmental use conditions, like voltage and temperature ranges, variations introduced in the manufacturing process, and the model inaccuracies. Safety margins are needed to ensure that everything works in the worst case. These margins hurt chip performance and the price the chip can bring. Reduction of these margins is a goal of the static timing methodology development.

Accurate modeling of the sources of variation in the timing flow allows to remove global margins and replace them with specific analysis of the circuit delay model. The characterization and modeling work required for this chip timing model is also costly and a lot of effort. Also the use in the timing tool adds to the complexity of the analysis. It is therefore important to focus on the variations with have the largest impact on the chip design timing.

The impact a specific source of variation has varies from circuit to circuit on the chip. But it is not only important to understand the effect on the circuit delay, but also the frequency with which this circuit is used.

In this Seminar I will explain these criteria and show examples on the metalization and interconnect timing how we can control and optimize the timing parameters used.