Chapter 12: Electrical Properties

Charge carriers and conduction:

Charge carriers include all species capable of transporting electrical charge, including electrons, ions, and electron holes. The latter are particularly important for describing the electrical behavior of semiconductors. Direct measurement of the ability of a material to conduct charge is provided by its resistance (R), which is described through Ohm’s law:

\[ V = IR \]

Obviously, I and V are the current and voltage, respectively. You all probably understand intuitively that if the length of a wire is doubled, then its resistance is also doubled. Similarly, if the diameter of a wire is reduced while the length is held constant, the resistance will increase. In other words, the resistance is an extrinsic property of the materials, meaning that its value depends on the amount of material present. We would like to understand electrical conduction through intrinsic properties, which depend only on the nature of the material, not the amount of that material. We can define the resistivity (\( \rho \)) according to:

\[ \rho = \frac{RA}{l} \]

where A is the cross-sectional area perpendicular to current flow and l is the length. The resistivity is an intrinsic material property, and some typical values are given in table 12.1.

<table>
<thead>
<tr>
<th>Metal</th>
<th>Electrical Conductivity ([\text{S} \cdot \text{m}^{-1}])</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silver</td>
<td>6.8 \times 10^7</td>
</tr>
<tr>
<td>Copper</td>
<td>6.0 \times 10^7</td>
</tr>
<tr>
<td>Gold</td>
<td>4.3 \times 10^7</td>
</tr>
<tr>
<td>Aluminum</td>
<td>3.8 \times 10^7</td>
</tr>
<tr>
<td>Brass (70 Cu–30 Zn)</td>
<td>1.6 \times 10^7</td>
</tr>
<tr>
<td>Iron</td>
<td>1.0 \times 10^7</td>
</tr>
<tr>
<td>Platinum</td>
<td>0.94 \times 10^7</td>
</tr>
<tr>
<td>Plain carbon steel</td>
<td>0.6 \times 10^7</td>
</tr>
<tr>
<td>Stainless steel</td>
<td>0.2 \times 10^7</td>
</tr>
</tbody>
</table>

Sometimes it is more convenient to use the conductivity (\( \sigma \)), another intrinsic material property defined as:

\[ \sigma = \frac{1}{\rho} \]
The conductivity is the product of several factors, the density of charge carriers \((n)\), the amount of charge \((e)\) each carrier possesses, and the inherent mobility \((\mu)\) of each carrier, assumed for now to be electrons. Thus the conductivity for most materials is:

\[
\sigma = ne\mu_e
\]

The carrier (electron) mobility \((\mu_e)\) quantifies the rapidity of motion of charge carriers in a potential gradient, in analogy to the diffusivity \((D)\), which measures the rapidity of motion of chemical species in a concentration gradient. The mathematics of transport that describes the motion of charge carriers is similar to that which describes the motion of chemical species.

**Energy levels and energy bands:**

In atoms, electrons occupy atomic orbitals with discrete energy levels. When atoms combine to form molecules, atomic orbitals interact and form “molecular” orbitals, which have different energies than the original atomic orbitals. This occurs due to the wavelike nature of electrons, which must obey the principles of quantum mechanics. Show figures 12.2 through 12.6.
Now imagine extending this principle to a Na solid containing $10^{23}$ Na atoms. In this case, the valence electron orbitals now overlap to form a very large number of closely spaced “bands” of electron orbitals. Since each of the 3s orbitals in individual Na atoms is only half-filled, the final 3s energy band is only half-filled. Each of these electron orbitals is delocalized throughout the Na solid, being shared among all of the Na atoms. At low room temperature, electrons can easily be thermally excited into unfilled electron orbitals in the upper half of the 3s energy band, allowing them to move in an electric field and conduct current. This corresponds to the situation shown in figure 12.4a.

Electrical conductivity in other metals is more complicated. In Mg, the 3s atomic orbital is completely filled, so the 3s energy band is also completely filled in Mg solid. However, this energy band overlaps energetically with another energy band that would otherwise be empty. This allows electrons from one band to be easily thermally excited into the other band, as illustrated in figure 12.4b.

Can we understand the electrical behavior of insulators (ceramics) using the same concept of energy bands? This is illustrated in figure 12.4c. In electrically insulating materials, such as most ceramics, the band gap ($E_g$) is large, so the upper energy band (conduction band) is unoccupied. When the band gap is large compared to thermal energies ($kT$), then thermal excitation of the conduction band is not feasible, and the material is an electrical insulator.

However, in semiconductor materials, $E_g$ is relatively small, so there is a small but not insignificant population of electrons in the conduction band, as illustrated in figure 12.4d. As a result, the electrical conductivity of a pure semiconductor is significantly less than that of a pure metal. However, unlike the case of metals, the electrical conductivity of semiconductors can be dramatically altered by changing the temperature or by introducing small amounts of impurities. The latter strategy has led to the development of the modern semiconductor industry. Note that for every electron promoted from the valence to the conduction band, a positively charged electron hole is created in the valence band. These holes serve as positively charged charge carriers.
Conductors:

In general, materials that are very good electrical conductors predominantly employ electrons as charge carriers. As mentioned above,

$$\sigma = n |e| \mu_e$$

where the subscript \(e\) refers to electron charge carriers. The resistivity of a metal is increased by any disruption in the regular crystalline lattice, which scatters electrons, as illustrated in Figure 12.7.

Such disruption can arise from the addition of impurity elements, from deformation associated with cold working, and from an increase in temperature, which both introduces vacancies and causes the atoms to vibrate away from their equilibrium lattice positions. Thus:

$$\rho_{total} = \rho_i + \rho_d$$

Show figure 12.8, which illustrates all these effects. In essence, all discontinuities in the crystalline lattice reduce the conductivity of metals. For example, since grain boundaries can reflect/deflect electron waves, the electrical conductivity of metals increases as the grain size increases. The increase in resistivity with temperature can be described according to:

$$\rho_i = \rho_0 + aT$$

where \(a\) is the temperature coefficient of resistivity.
Show figure 12.9, which illustrates the linear relationship between \( \rho \) and impurity concentration, at low impurity concentrations. More generally:

\[
\rho_i = A c_i (1 - c_i)
\]

where A is a composition-independent constant.
**Example Problem:**

A tungsten light bulb filament is 9 mm long and 10 µm in diameter. What is the current in the filament when operating at 1000°C with a line voltage of 110 V? Here \( \rho_0 = -17.5 \times 10^{-9} \ \Omega \cdot m \) and \( a = 2.48 \times 10^{-10} \ \Omega \cdot m/°K \).

Reading this problem carefully, we are really being asked to determine the resistance/resistivity of the tungsten filament at 1000°C. If we know the filament resistance and line voltage, current calculation follows trivially from Ohm’s law. We know that:

\[
\rho_t = \rho_0 + aT
\]

\[
\rho(1000°C) = -17.5 \times 10^{-9} \ \Omega \cdot m + \left(2.48 \times 10^{-10} \ \Omega \cdot m/°K \right) (1273°K)
\]

\[
\rho(1000°C) = 2.98 \times 10^{-7} \ \Omega \cdot m
\]

If you instead do this calculation at room temperature, \( \rho(20 °C) = 5.51 \times 10^8 \ \Omega \cdot m \). Note that the resistivity is > 5x higher than at room temperature!! Now from Ohm’s law and the definition of resistivity:

\[
I = \frac{V}{R} = \frac{VA}{\rho l}
\]
Research and Development Example: Cu in Integrated Circuits:

Gordon Moore is one of the co-founders of Intel, and he predicted in 1965 that the number of transistors on an integrated circuit would double every two years. This is the now known as Moore’s law, and is the economic foundation of the semiconductor industry. Doubling the number of transistors every two years simultaneously yields increasing performance AND decreasing cost. From a manufacturing perspective, Moore’s law REQUIRES continuously decreasing device dimensions. In 2011, the semiconductor industry is using the 22 nm node in their most advanced devices. The 1st Figure below shows a CMOS device schematic. The dimensions of the following materials are all gradually reduced:

- Gate insulator (SiO$_2$ here, but new materials under development)
- Electrical connections to the source, gate and drain (Al, W or Cu)
- p-type wells below source and drain. These were originally created by diffusion processes, but are now created by ion implantation. Following ion implantation, the damaged Si surface is annealed to “activate” the p-type dopants. This process involves both diffusion and recrystallization of the damaged Si.

Moore’s law is illustrated by the two Figures below.
In the late 1990's, Cu began to replace Al as the material for interconnect wires in
integrated circuits, or semiconductor devices, including cpu and DRAM chips in computers, chips in home electronics, and chips in communications devices (cell phones, cable modems, etc.). The Figure below shows a CMOS-based integrated circuit from IBM. On the left, all the parallel lines are Cu interconnect wires, like you have seen before in electron microscope images of semiconductor chips. Choosing the best material for the interconnect wires, and choosing the best wiring scheme, have been areas of enormous R&D investment in the semiconductor industry.

If you inspect Table 12.1, the two common metals with the lowest $\rho$ are Al and Cu. Ag has the lowest $\rho$, but is expensive for industrial production, and suffers from electromigration. Originally, Al was used for interconnect wires in computer and other semiconductor chips because it is easier to pattern than Cu, and it is cheaper than the other low-$\rho$ metals. The Al was patterned by depositing a continuous Al film on the wafer surface, and Al was then etched away from the unwanted regions.

Eventually, the Al wires had such a small cross-sectional area that their resistance became too high. In addition, the Al wires began to fail by electromigration, where the electron flow causes momentum transfer to Al atoms, eventually forming voids in the Al wires. During the early 1990’s, researchers predicted that Al must eventually be replaced by Cu, and they began to study how to do this. Planning in the semiconductor industry is coordinated through the International Technology Roadmap for Semiconductors (ITRS), http://www.itrs.org. Unlike Al, Cu cannot be effectively chemically etched, so new technologies were developed. Cu interconnect wires in the above figure were fabricated by a subtractive Damascene process, named for its use in ancient Damascus for making inlaid patterns of precious metals for jewelry. In the Damascene process, the Cu wiring pattern is first etched into an electrical insulator, these trenches are then filled with Cu by electrodeposition, and the excess Cu is polished away by chemical mechanical planarization (CMP). Clarkson has perhaps the world's leading research program in CMP and hosts an international CMP symposium each August in Lake Placid. More information is available online at

http://people.clarkson.edu/projects/thinfilm//CMP/Cmp1.html

The Damascene process is shown below:
An additional complication of Cu interconnect wiring is that most advanced integrated circuits are multi-level devices. As a result, wire lengths can become very long. This has required the use of “fat” wiring, shown in the next Figure below, where each successive wiring layer has wires with larger cross-sectional areas.

**RC circuit delay**

The networks of resistors and capacitors in integrated circuits have an associated RC circuit delay that limits the speed at which this network can carry electrical signals. This is determined by a mixture of design parameters (dimensions of wires and capacitors) and materials properties (resistivity and dielectric constant):

\[ RC = \frac{\rho_{\text{met}} \varepsilon_{\text{ox}} L^2}{t_{\text{met}} t_{\text{ox}}} \]

In this equation, there are two fundamental material properties, the metal (Cu or Al) resistivity (\( \rho_{\text{met}} \)) and is the insulator (SiO\(_2\) or porous replacement) dielectric constant (\( \varepsilon_{\text{ox}} \)). The other parameters arise from device design, including L (wire length), \( t_{\text{met}} \) (thickness or width of metal wires), and \( t_{\text{ox}} \) (thickness or width of dielectric insulator).
This illustrates the materials challenges that are created as devices dimensions \( (t_{\text{met}}, t_{\text{ox}}) \) are continuously reduced according to Moore’s law. These reductions in device size cause an increase in the RC time constant. This requires the introduction of metals with lower resistivity (Al replaced by Cu) and dielectric spacing materials with lower dielectric constant (SiO\(_2\) replaced by polymers, then by porous SiO\(_2\)/polymers). Currently, intensive research is ongoing in semiconductor companies into porous low dielectric constant spacer materials.

**Semiconductor Materials:**

Many pure solid elements and compounds (Si, Ge, GaAs, InP, etc.) are classified as semiconductors. As discussed in section 12.5, this means that they are intermediate between metals (zero band gap) and insulators (very high band gap). Pure semiconductor materials exhibit relatively low conductivities (still much higher than insulators), but the utility of these materials is that the electrical properties can be modified very dramatically by the introduction of controlled, small amounts of impurities. The properties of some common semiconductor materials are given in Table 12.3 below.
Intrinsic, elemental semiconductors:

Pure elemental semiconductors have equal numbers of electrons and electron holes because every electron that is thermally excited to the conduction band leaves behind an electron hole in the valence band. Show figure 12.11 (at right). Electrical current can be carried either by electrons (conduction band) or by electron holes (valence band). The conduction band electrons are delocalized over the entire crystalline solid, as in metals. However, the valence electrons are associated with specific covalent bonds, so electrical conduction by electron holes requires electrons from an adjacent covalent bond to hop into an empty electron hole. A coordinated series of such hops in the direction of the applied electric field will carry electrical current. The hopping of electrons to fill electron holes is similar to the hopping of atoms to fill vacancies during solid-state diffusion. Although the species moving are actually electrons, this is easier to visualize as hopping of the electron holes in the opposite direction.

Therefore, the conductivity of an intrinsic, elemental semiconductor is:

$$\sigma = n |e| \mu_e + p |e| \mu_h$$

where $n$ is the electron concentration, $p$ is the hole concentration, and $\mu_e$ and $\mu_h$ are the electron and hole mobility, respectively. However, each thermal activation event produces 1 electron and 1 electron
hole, so \( n = p = n_i \) for an intrinsic semiconductor. In addition, the absolute value of the charge carried by each of these carriers is the same:

\[
\sigma = n_i |e| (\mu_e + \mu_h)
\]

Show Figure 12.16 below, which illustrates the temperature dependence of the carrier concentration. This is poorly plotted, since it follows an Arrhenius type equation:

\[
n_i \propto \exp \left( -\frac{E_g}{2kT} \right)
\]

\[
\ln n_i \propto -\frac{E_g}{2kT}
\]

The extra factor of 2 in the denominator because 2 charge carriers are created for every thermal excitation.

The exponential increase in carrier concentration with temperature causes a corresponding increase in the conductivity with temperature for an intrinsic semiconductor. However, the carrier mobility is typically reduced as the temperature increases, as shown in Figure 12.19 below. Buried within problem 12.17 is an equation for the temperature dependence of the conductivity of Ge:
\[ \sigma = C T^{-3/2} \exp \left( - \frac{E_g}{2kT} \right) \]

In general, the contribution of the exponential factor (thermal population of electron-hole pairs) is much greater than the contribution of the \( T^{-3/2} \) factor (reduced mobility with increased temperature), so the latter is sometimes ignored.
Example Problem:

Starting from an ambient temperature of 300 K, what temperature increase is necessary to double the conductivity of pure Ge? For the sake of simplicity, assume that temperature affects only the carrier concentration, not the electron and hole mobilities.

If the only effect of temperature is on the carrier concentration, we can write that:

$$\sigma = \sigma_0 \exp \left( -\frac{E_g}{2kT} \right)$$

Take the Arrhenius form of this equation for two temperatures, ambient temperature and that which doubles the conductivity, and divide them:

$$\frac{\sigma(T_1)}{\sigma(T_2)} = \frac{\sigma_0 e^{-E_g/2kT_1}}{\sigma_0 e^{-E_g/2kT_2}} = e^{\frac{E_g}{2k}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)}$$

$$\ln \left[ \frac{\sigma(T_1)}{\sigma(T_2)} \right] = \frac{E_g}{2k} \left( \frac{1}{T_2} - \frac{1}{T_1} \right)$$

$$\ln 2 = \frac{0.67 \text{eV}}{2(8.62 \times 10^{-5} \text{ eV/K})} \left( \frac{1}{300 \text{K}} - \frac{1}{T_1} \right)$$

$$\frac{1}{300 \text{K}} - \frac{1}{T_1} = 1.784 \times 10^{-4} / \text{K}$$

$$T_1 = 317 \text{ K}$$

Notice that the conductivity doubles from only a 17ºK rise in temperature.

If we take into account the possible T^{-3/2} factor, then this problem can only be solved by trial and error. In many cases, it is easier to include only the exponential factor, and the answer that is obtained is still reasonably accurate. Note here that $(317/300)^{1.5} = 0.92$, so this effect is much smaller than the exponential effect due to carrier concentration.

**Extrinsic, elemental semiconductors:**

Extrinsic semiconductors are formed by deliberate addition of specific impurity elements (dopants) to a pure semiconductor material. The addition of Group V elements, which have one extra valence electron than Si and Ge, creates n-type semiconductors. Four of the five electrons in Group V elements (P, As, Sb) are used to create local bonds to
adjacent Si atoms. The 5\textsuperscript{th} electron is not needed for bonding and produces a donor level near the conduction band, which is much easier to thermally activate into the conduction band than valence electrons. Show figure 12.12 (at right). The result is that electrons far outnumber electron holes, and the conductivity of an n-type semiconductor is:

$$\sigma = n |e| \mu_e$$

The addition of Group III elements, which have one less valence electron than Si and Ge, creates p-type semiconductors. All three electrons in Group III elements (Al, Ga, In) are used to create local bonds to adjacent Si atoms, but four bonds are needed to adjacent Si atoms. This results in the creation of an acceptor level near the valence band of Si, as shown in figure 12.14 below, that is relatively easy to thermally populate from the valence band. The result is that electron holes far outnumber electrons, and the conductivity of a p-type semiconductor is:

$$\sigma = p |e| \mu_h$$

Discuss qualitatively the dependence of carrier concentration on temperature, and the factors that influence carrier mobility. Show figure 12.17 (on next page).
Effect of dopant concentration on electrical conductivity:

Here is a simple model calculation to illustrate how dramatically the addition of dopant elements increases the electrical conductivity of Si, and other semiconductors. The electron concentration \( n \) in an n-type semiconductor is roughly equal to the concentration of n-type doping elements that are added. Therefore, we can calculate the increase in conductivity with the concentration of n-type dopant. For intrinsic (pure) Si at room temperature, Table 12.3 gives the room-temperature conductivity \( \sigma \) as \( 4 \times 10^{-4} \, (\Omega \cdot m)^{-1} \). With addition of 0.001 atom\% As, assuming that all the extra electrons are activated into the conduction band:

\[
\begin{align*}
  n_{Si} &= \frac{8 \text{ atoms}}{a^3} = \frac{8 \text{ atoms}}{(8R)^3} = \frac{3\sqrt{3}}{64R^3} \\
  n_{Si} &= \frac{3\sqrt{3}}{64(0.118 \times 10^{-9} \text{ m})^3} = 4.94 \times 10^{28} \text{ m}^{-3}
\end{align*}
\]
For 0.001 atom% As,

\[ n_{As} = 10^{-5} \left( 4.94 \times 10^{28} \text{ m}^{-3} \right) = 4.94 \times 10^{23} \text{ m}^{-3} \]

Looking up the electron mobility from Table 12.3:

\[ \sigma = n |e| \mu_c \]

\[ \sigma = \left( 4.94 \times 10^{23} \text{ m}^{-3} \right) \left( 1.602 \times 10^{-19} \text{ C} \right) \left( 0.140 \text{ m}^2 / \text{V} \cdot \text{sec} \right) \]

\[ \sigma = 1.1 \times 10^4 \text{ } \Omega^{-1} \text{ m}^{-1} \]

A small level of impurity (0.001 atom%) increases the conductivity by 8 orders of magnitude!! The ability to tune the electrical properties of semiconductors is what makes semiconductor devices possible. We have not considered whether or not As is sufficiently soluble in Si. Does it have the same crystal structure, similar atomic radius, similar valance and electronegativity? As almost certainly fails this test, but this does not matter, given the low concentration (0.001 atom%) of As. If you inspect any of the phase diagrams in Chapter 10, the solubility limit of even relatively insoluble materials is usually not below 0.001 atom%.

How do transistors work?

In the 21st century, one might argue that all educated people should understand how a transistor works. The main components of a transistor are p-n junctions, which are typically rectifying, meaning that they behave like diodes, carrying current in one direction only. A p-n junction is a region where a p-type semiconductor borders with an n-semiconductor. This is illustrated schematically in Figure 12.21 of the textbook below.
Under a forward bias, electrons are repelled from the negative terminal and attracted by the positive terminal, directing them through the p-n junction. Holes experience the opposite forces, but are also directed through the p-n junction. On the other hand, under reverse bias, electrons and holes are both drawn away from the p-n junction, leaving this region bereft of charge carriers. As a result, the p-n junction is only “conductive” under forward bias, so its i-V behavior is shown in Figure 12.22 below. The p-n junction behaves like a diode (rectifier), not a resistor.
Most transistors are now metal oxide semiconductor field effect transistors (MOSFET), as shown in Figure 12.26 below, p-channel MOSFET device.

In a MOSFET, two p-n junctions of opposite polarity are created by forming two p-doped (n-doped) wells to form a p-channel (n-channel) MOSFET. In either case, the material between the two wells that are formed contains dopant of the opposite type. Since the two p-n junctions are of opposite polarity, the transistor will not carry current when it is off. In other words, if no potential is applied to the gate, the resistance between the source and drain is quite high for an applied voltage of either polarity. However, if a
large enough negative potential is applied to the gate electrode of a p-channel device, the negative potential can penetrate through the thin gate dielectric, repelling electrons from the region near the gate. This creates a thin channel near the gate that the applied potential has converted from n-type to p-type. The p-channel region that is formed creates a continuous p-type pathway between the source and drain. Now the transistor is conducting, and current can flow between the source and drain. This is a simple method for making a binary switch (logic gate), or an amplifier. By connecting many transistors in a logic circuit, complicated integrated circuits can be fabricated.

Note that the transistor shown in Figure 12.26 is fabricated by surface engineering. The n-type Si substrate is about 1 mm thick, but the p-type dopant wells are about 100 nm deep, and the gate oxide is perhaps 1-2 nm thick. Most of the thickness of the Si wafer is not involved in the actual transistor, but provides mechanical support so that the transistor is not broken easily. Traditionally, the p-type dopant wells were created by diffusion of p-type dopants (Al, Ga, In) inside the Si wafer. As we learned in Chapter 6, diffusion over a 100 nm length scale is much more rapid than diffusion over a 1 mm length scale, illustrating why the transistor is created only in the surface layer. Diffusion has been gradually replaced by ion implantation for many applications, since this allows better control over the exact distribution of the dopant element within the Si wafer.

For more information about CMOS transistors and how they work, see the information available at [www.wikipedia.org](http://www.wikipedia.org) and [www.howstuffworks.com](http://www.howstuffworks.com). See, for example: