EE 264
Hour Exam II

Name: ______________________
Student Number: ____________

1. (a) (1.5 points) Implement the following logic expression using only NAND gates.
   \[ X = \overline{A} \cdot (B + C \cdot (\overline{D} + E)) \]

   (b) (1.5 points) Repeat (a) using only NOR gates.
2. (3 points) Determine the Q output waveform if the inputs shown below are applied to a gated S-R latch that is initially SET.

(a) Logic diagram
(b) Logic symbol

3. (3 points) A J-K flip-flop and associated waveform are shown in figure below. Draw the output Q. Assume that the flip-flop is initially RESET.
4. (3 points) The waveforms below are applied to a gated D-latch and a positive edge-triggered D-Flip-flop. Determine the Q outputs waveform for the gated latch Q (latch) and the D- positive edge-triggered D-flip-flop Q (FF). Assume the latch and the FF is both in the RESET state at the beginning.

5. (3 points) Using only one 4:1 MUX (4-input data selectors) design a Boolean function expressed as: \( H(Y,X,W) = \Sigma m(0,1,3,6,7). \)
6. (5 Points) A logic circuit has two 4-bit words \(X = X_3X_2X_1X_0\) and \(Y = Y_3Y_2Y_1Y_0\) as inputs and two 1 bit outputs \(W\) and \(Z\). Design the logic circuit such that \(W = 1\) when only when an even number of the following conditions is true and \(Z = 1\) when only two of the three are true:

- \(X_1\) is not equal to \(Y_3 \oplus X_1\)
- \(X_2 \oplus X_3\) is equal to \((Y_1 \cdot X_0) \oplus Y_2\)
- \(X_0\) is equal to \((X_3 + Y_2)\)

\[
W = \overline{A \oplus B \oplus C}
\]

\[
3 = (A \cdot B \cdot C) + (A \cdot \overline{B} \cdot C) + (A \cdot B \cdot \overline{C})
\]
7. (5 Points) The following VHDL files are contained in a Qurtus II project. Draw the gate level schematic diagram for the logic circuit. Label all the inputs and gates. Complete the expected simulation result for the project.

```
library ieee;
use ieee.std_logic_1164.all;

entity myINV is
    port ( 
        A : in  std_logic;
        F : out std_logic
    );
end myINV;

architecture dataflow of myINV is
begin
    F <= not A;
end dataflow;

library ieee;
use ieee.std_logic_1164.all;

entity myOR2 is
    port ( 
        A : in  std_logic;
        B : in  std_logic;
        F : out std_logic
    );
end myOR2;

architecture dataflow of myOR2 is
begin
    F <= A or B;
end dataflow;

library ieee;
use ieee.std_logic_1164.all;

entity myAND2 is
    port ( 
        A : in  std_logic;
        B : in  std_logic;
        F : out std_logic
    );
end myAND2;
```
architecture dataflow of myAND2 is
begin
    F <= A and B;
end dataflow;
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library ieee;
use ieee.std_logic_1164.all;

entity toplevel is
port (
    A    : in std_logic;
    B    : in std_logic;
    C    : in std_logic;
    X    : out std_logic
);
end toplevel;

architecture structural of toplevel is

component myOR2 is
port (
    A    : in std_logic;
    B    : in std_logic;
    F    : out std_logic
);
end component myOR2;

component myAND2 is
port (
    A    : in std_logic;
    B    : in std_logic;
    F    : out std_logic
);
end component myAND2;

component myINV is
port (    A    : in std_logic;
            F    : out std_logic
);
end component myINV;
Signal ABAR, BBAR, CBAR, OUT1, OUT2, OUT3, OUT4: std_logic;
begin
G1: myINV port map(A=>A, F=>ABAR);
G2: myINV port map(A=>B, F=>BBAR);
G3: myINV port map(A=>C, F=>CBAR);
G4: myAND2 port map(A=>ABAR, B=>BBAR, F=>OUT1);
G5: myAND2 port map(A=>OUT1, B=>CBAR, F=>OUT2);
G6: myAND2 port map(A=>ABAR, B=>B, F=>OUT3);
G7: myAND2 port map(A=>OUT3, B=>C, F=>OUT4);
G8: myOR2 port map(A=>OUT2, B=>OUT4, F=>X);
end structural;

\[
\begin{align*}
\text{ABAR} &= \bar{A} \\
\text{BBAR} &= \bar{B} \\
\text{CBAR} &= \bar{C} \\
\text{out1} &= \bar{A} \cdot \bar{B} \\
\text{out2} &= (\bar{A} \cdot \bar{B} \cdot \bar{C}) \\
\text{out3} &= \bar{A} \cdot \bar{B} \cdot C \\
\text{out4} &= (\bar{A} \cdot \bar{B} \cdot \bar{C}) \\
X &= (\bar{A} \cdot \bar{B} \cdot \bar{C}) + (\bar{A} \cdot \bar{B} \cdot C)
\end{align*}
\]

\[
X(A, B, C) = \sum m(0, 3)
\]