Solution to HW #8
EE 264  Introduction to Digital Design

9-1

9-4 (b)

74 LS93 A

Modulo-11 Counter

Counter must be "cleared" as soon as reaches $11_{10} = Q_3Q_2Q_1Q_0 = 1011$

9-8
This problem is not really correct. CTEN & LOAD should not change until the negative edge of the CLK.

I will assume that these changes take place "before" the negative edge of the clock.

\[ 0110 \]

\[ \text{CLK} \]
\[ \text{CTEN} \]
\[ \text{LOAD} \]
\[ Q_0 \]
\[ Q_1 \]
\[ Q_2 \]
\[ Q_3 \]

\[ \text{TC} \]

\[ \text{High when } Q_2 \ldots Q_0 \text{ reaches 111} \]
9-14

Present State: \( Q_2 \ Q_1 \ Q_0 \)
Next State: \( Q_2^* \ Q_1^* \ Q_0^* = D_2 \ D_1 \ D_0 \)

State Equations:
\[
\begin{align*}
D_2 &= Q_1 \\
D_1 &= Q_0 \\
D_0 &= Q_2 \cdot Q_1
\end{align*}
\]

Initially:

<table>
<thead>
<tr>
<th>( Q_2 \ Q_1 \ Q_0 )</th>
<th>( D_2 \ D_1 \ D_0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>0 0 1</td>
</tr>
<tr>
<td>0 0 1</td>
<td>0 1 1</td>
</tr>
<tr>
<td>0 1 1</td>
<td>1 1 1</td>
</tr>
<tr>
<td>1 1 1</td>
<td>1 1 0</td>
</tr>
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</tr>
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<td>0 0 1</td>
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</tr>
</tbody>
</table>

Sequence:
\( 0 \rightarrow 1 \rightarrow 3 \rightarrow 7 \rightarrow 6 \rightarrow 4 \)

"The sequence repeats"

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State Diagram

\[
\begin{array}{c}
00 \\
\downarrow \\
11 \\
\uparrow \\
10
\end{array}
\]
Need 2 J-K FFs. \( \text{State} = Q_1Q_0 \)

Note \( \text{state} \) is also the output

**Flip-flop Transition Table**

<table>
<thead>
<tr>
<th>Output Transitions</th>
<th>Flip-Flop Inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>( Q_n )</td>
<td>( Q_{n+1} )</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**State Table**

<table>
<thead>
<tr>
<th>Present State ( Q_1Q_0 )</th>
<th>Next State ( Q_1'Q_0' )</th>
<th>( J_1 )</th>
<th>( K_1 )</th>
<th>( J_0 )</th>
<th>( K_0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>10</td>
<td>1</td>
<td>X</td>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>0 1</td>
<td>11</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>1 0</td>
<td>01</td>
<td>1</td>
<td>X</td>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1 1</td>
<td>00</td>
<td>1</td>
<td>X</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**K-maps**

\( J_1 = 1 \)

\( K_1 = 1 \)

\( J_0 = Q_1 \)

\( K_0 = Q_1 \)
Counter Implementation

![Diagram of a counter circuit with state transitions labeled as Q-18 to Q-5.]

Repeats

Since the counter's highest output value is 9, we need 4 Flipflops.

State = Counter output = Q_3Q_2Q_1Q_0

State Table

<table>
<thead>
<tr>
<th>Reset Q_3Q_2Q_1Q_0</th>
<th>Next Q_3Q_2Q_1Q_0</th>
<th>J_3 K_3</th>
<th>J_2 K_2</th>
<th>J_1 K_1 J_0 K_0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0</td>
<td>1 0 0 1</td>
<td>1 x</td>
<td>0 x</td>
<td>0 x</td>
</tr>
<tr>
<td>0 0 0 1</td>
<td>1 0 0 0</td>
<td>1 x</td>
<td>0 x</td>
<td>0 x</td>
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<td>0 1 1 1</td>
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<td>0 x</td>
</tr>
</tbody>
</table>
$J_3 = \overline{Q}_2 \cdot \overline{Q}_1$

$K_3 = 1$

$J_2 = Q_1$

$K_2 = Q_6$

$J_1$

$K_1$
\[ J_1 = Q_3 \cdot \overline{Q}_0 \]

\[ K_1 = Q_2 \cdot \overline{Q}_0 \]

\[ J_0 = (\overline{Q}_3 \cdot \overline{Q}_2) + (Q_3 \cdot \overline{Q}_1) \]

\[ K_0 = (\overline{Q}_3 \cdot \overline{Q}_2) + (Q_3 \cdot \overline{Q}_1) \]

**Implementation:**

\[ \overline{Q}_2 \quad \overline{Q}_1 \]

\[ \overline{Q}_2 \quad \overline{Q}_1 \]

\[ Q_2 \quad Q_1 \quad Q_0 \]

\[ Q_2 \quad Q_1 \quad Q_0 \]

\[ J_3 \quad Q_3 \]

\[ J_2 \quad Q_2 \]

\[ J_1 \quad Q_1 \]

\[ J_0 \quad Q_0 \]

\[ K_3 \quad \overline{Q}_3 \]

\[ K_2 \quad \overline{Q}_2 \]

\[ K_1 \quad \overline{Q}_1 \]

\[ K_0 \quad \overline{Q}_0 \]
20 (d) \[ \text{Modulus} = 2 \times 4 \times 6 \times 8 \times 16 = 6144 \]

\[
\begin{align*}
f_1 &= \frac{39.4 \text{ kHz}}{2} = 19.7 \text{ kHz} \\
f_2 &= \frac{19.7 \text{ kHz}}{4} = 4.925 \text{ kHz} \\
f_3 &= \frac{4.925 \text{ kHz}}{6} = 0.820 \text{ kHz} \\
f_4 &= \frac{8.20 \text{ kHz}}{8} = 1.026 \text{ kHz} \\
f_5 &= \frac{16.26 \text{ kHz}}{16} = 0.414 \text{ kHz}
\end{align*}
\]