

Modeling and Performance of a SRM Drive with Improved Ride-Through Capability

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Abstract—One of the problems with the switched reluctance motor drive, which is a problem of increasing concern for all drives, is the ability to ride through dips or short duration power outages of several power cycles. In this paper, the modeling and performance of a chopper controlled SRM drive is presented with the aim of improving its ride-through capability. Super capacitors are used in the power supplies of the driver and logic circuits to allow them to operate in the absence of mains power. Practical measurements of the improved ride-through capability are included.

I. INTRODUCTION

THE SWITCHED reluctance motor (SRM) has considerable potential for industrial applications because of its high reliability as a result of the absence of rotor windings. In addition, most of the losses are confined to the stator from where they are more easily removed. The SRM is thus more robust both thermally and mechanically, than a squirrel-cage induction motor [1]–[3]. One of the problems of increasing concern for all drives is the ability to ride-through dips or short duration power outages of several power cycles.

Most of the current drives on the market have instantaneous trips for undervoltage. Voltage spikes, thus produce nuisance tripping. At the same time, drives are being used in more critical applications because of the improved performance they provide. The industry, and in particular the continuous process industry is concerned about the ability of motors and drives to ride through short term outages or voltage dips [4]. The loss of a critical motor or drive can cause expensive downtime and hours or even days are sometimes required before full production is achieved again.

In this paper, a chopper is placed in series with the rectifier and dc link capacitor to improve the ride through capability. The use of the chopper also allows controlled charging of the dc link capacitors during startup and thus avoids the use of a charging circuit. Particular attention is paid to providing power to the electronics and driver circuits during power interruptions so that they are operational during the outage as well as providing the ability to detect and reapply the mains power to the motor in a controlled manner.

The paper is organized into 5 sections. Section II discusses modification to the drive design to improve the ride through capability. Section III presents a brief model of the SRM.

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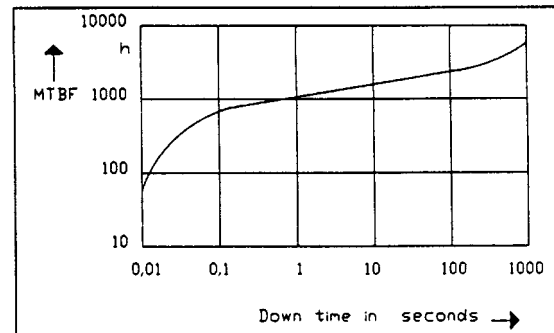


Fig. 1. Mean time between failures (MTBF) versus down time of the public power supply [4].

Section IV discusses the modeling of the rectifier and its different conduction sequences. Section V presents computer simulation as well as experimental results while Section VI has the conclusions.

II. DRIVE DESIGN FOR IMPROVED RIDE-THROUGH CAPABILITY

A. Introduction

Motor drives are notorious for their low tolerance to supply disturbances. Many have instantaneous trips that disconnect the drive from the supply for an undervoltage of say 90% of the nominal. Thus, a negative voltage spike of short duration may disconnect the drive, resulting in nuisance tripping.

Fig. 1 indicates that a power interruption of 10 ms duration is likely to occur every 80 h on the average. On the other hand, the mean time between failures (MTBF) for the power converters are of the order of 10 000 hours. Short time interruptions of the power supply are therefore the most frequent cause for inverter tripping [4].

The commercial SRM drive used in this paper utilizes a series resistor to control the charging current of the dc link capacitor. Once the dc link reaches the nominal operating voltage, the resistor is shorted with a relay.

During a supply disturbance like an outage for a few cycles or a dip for several cycles, the dc link voltage will rapidly reduce as it supplies power to the motor. In the commercial drive, the entire drive is disconnected at around 90% of nominal voltage. The reason is that if the power is reclosed onto a low dc link voltage, a large surge in the rectifier current will result, which can easily exceed the diode ratings.

Thus, to improve the ride-through capability, either the series resistor must be reinserted at some defined dc link voltage or an alternative technique used to control the inrush current. An

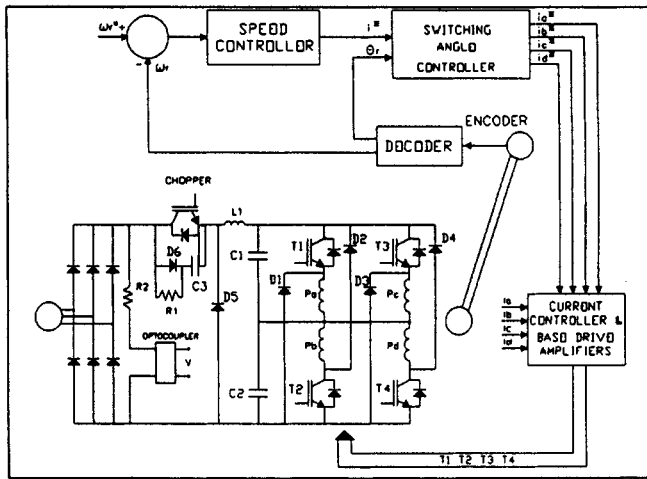


Fig. 2. Block diagram of the DSP based control system a DSP.

alternative is to use a chopper which can control the inrush current by varying the mark-space ratio. Thus, the input voltage can be matched to the residual dc link voltage (on the output of the chopper) with a proper mark-space ratio.

B. Super Capacitors

Super capacitors, also known as Double Layer Capacitors (DLCs), are a new electric energy storage device with extremely high volumetric efficiency (over three farads/in³), virtually unlimited service life, fast charge/discharge capability and very low leakage current [5]. The commercial names for these capacitors are: super capacitors, ultra capacitors or capattery. The generic name is double layer capacitor.

Conventional energy storage devices such as batteries and aluminum electrolytic capacitors often must be replaced during the life of a product. Super capacitors last much longer because unlike batteries, they do not undergo life-limiting, irreversible chemical reactions, and unlike aluminum electrolytic capacitors, they do not experience dry-up problems.

C. Overall Block Diagram

The motor drive consists of the speed, switching angle and current feedback controllers as well as the rectifier, chopper, split-link converter, motor and encoder as is shown in Fig. 2 [6]. Speed and position feedback are obtained from an absolute optical encoder. The commanded speed ω_r^* is compared with the actual speed ω_r ; the difference between these two signals is the speed error. This error is the input of a PI speed controller. The output of the PI controller is the commanded torque from which a current " i^* " is produced.

The switching angle controller produces the reference currents $i_a^*, i_b^*, i_c^*, i_d^*$, the rotor position θ_r , and i^* . These are compared with the actual $i_a, i_b, i_c,$ and i_d currents for current control. While many different forms of current control are available, a simple hysteresis controller is used here. The actual i_a, i_b, i_c and i_d currents are measured using current transducers.

Some overlap between the phase currents is often desirable to minimize the torque ripple; this overlap is achieved by advancing the firing angle of each phase and is controlled by a DSP. The motor used is a commercial SRM with 8 stator poles and 6 rotor poles.

The rectifier is supplied from a 3-phase 460 V AC supply. It converts this voltage to a 600 V DC supply. The constant DC supply from the rectifier is then converted to a variable DC supply by means of a series chopper. The chopper operates at 5 kHz frequency and varies the input voltage to the SRM converter based on the speed. There is an L-C filter between the chopper and the converter to smooth the current waveform input to the split-link converter, which supplies power to different windings of the SRM stator depending on the rotor position.

The rotor position is sensed by an optical encoder mounted on the shaft of the motor. Depending on the rotor position, the control circuit generates firing signals for a particular phase of the stator winding. This signal is amplified and isolated from the converter (Power Circuit) by the driver circuit. The control signal is passed to the converter IGBTs via the driver circuit. The split link converter allows the use of 4 power switching devices with 4 phases and only 2 current transducers.

D. Power Circuit

In this converter, $T1$ is used to allow current to flow into phase 1. For current control, $T1$ is turned off and the current freewheels through $D1$, capacitor $C2$ and phase 1. When the current flows through $C2$, $-1/2$ Vdc is effectively applied to phase 1 so that the current reduces more quickly than if 0 V is applied. In order to turn the phase off completely, $T1$ is turned off and the current takes the same path as during freewheeling so that the rate of fall is the same as during current control.

E. Enhancements of the Semicron Driver Circuits to Improve the Ride-Through Capability

Up to now, a conventional drive design has been described. The power supply discussed here is the 15 Volts floating power supply designed for the driver circuit. In order to improve the ride-through capability of the driver circuits, super capacitors are connected on the output. To ensure the voltage across individual devices in the series string does not exceed the maximum voltage of each capacitor, zener diodes are connected in parallel to each super capacitor. The value of the super capacitors chosen for the drive power supply was determined experimentally to provide the desired output voltage for a 15 cycle interruption. The value is 1.1 F. Three 5.5 V super capacitor were used in series because of the availability of the 5.5 V rating. As higher voltage supercapacitors become available, they could be used in the dc link as well.

The drivers used for the chopper and for the four switches $T1$ to $T4$ are the SKHI 21 manufactured by SEMIKRON. Each driver controls two IGBTs, so only three drivers are required. The power supply for these drivers is 15 V. The supply current is 160 mA. The minimum supply voltage is 13 V. If it falls below this value the turn-on pulses for the IGBTs are blocked. The

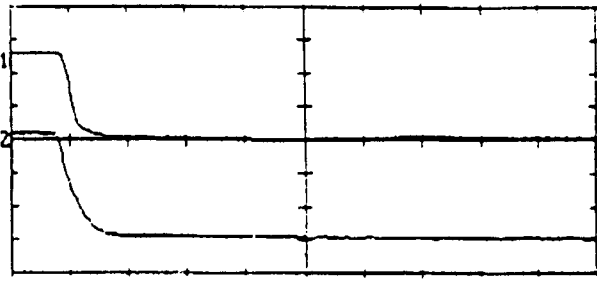


Fig. 3. 5 V and 15 V supply voltage without super capacitors. 2 V/div (top), 5 V/div (lower). 0.1 s/div.

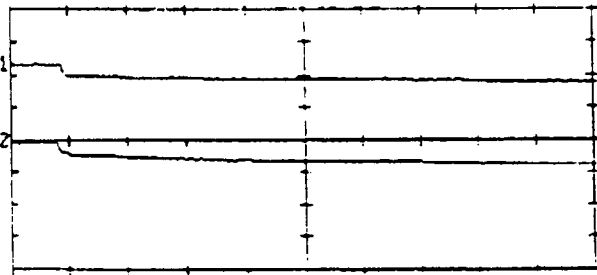


Fig. 4. 5 V and 15 V supply voltage with super capacitors. 2 V/div (top), 5 V/div (lower). 0.2 s/div.

voltage of the super capacitors during the power interruption must be greater than 13 V.

F. Super Capacitors for the Logic Circuit

The DSP TMS320E15 and all the logic requires 5 V DC and the supply current is 1.3 amps. Hence four super capacitors rated at 3.3 F, 5.5 V are used to provide standby power. The current transducers, the analog to digital converter and the analog switch requires +12 V DC and -12 V DC and the supply current is 130 mA. Thus three super capacitors of 3.3 F 5.5 V DC connected in series are used to provide backup power. To ensure equal voltage distribution, 5.6 V zener diodes are connected across each capacitor. The discharge rates of the 5 V logic, as well as the +15 V supply, both with and without super capacitors are in Figs. 3 and 4, respectively.

G. Algorithm for Improved Ride-Through Capability

During a power interruption or dip, the chopper is turned off, but the controller continues firing the phases through the converter, based on the rotor position. Because the chopper is off, there is no current flow from the power supply, and the dc link capacitors supply energy to the motor. The energy stored in the dc link capacitors is relatively small, therefore the capacitor voltage decays. Hence the speed also decays, since the motor energy requirements are not being met.

Fig. 5 gives the algorithm for improved ride through capability during the power interruption or dip. To detect the interruption or dip in the power supply, a resistor $R2 = 100K$ and an optocoupler LM3093 IC9 are connected as shown in Fig. 2. A current i flows through the resistor and the optocoupler. A voltage V proportional to the current i appears at the output of

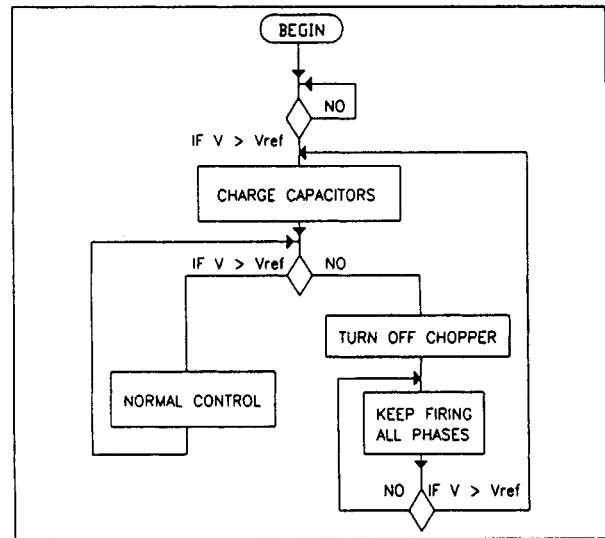


Fig. 5. Logic used to improve the ride through capability during power interruption or dip of the input voltage.

the optocoupler. Hence the voltage V is also proportional to the dc link voltage at the output of the bridge rectifier.

The voltage V , is compared to a reference voltage V_{ref} . When $V > V_{ref}$ the output of the comparator is low. If $V < V_{ref}$ the comparator output goes high; under this condition a dip or an interruption in the power supply has been detected. To avoid oscillations, the output of the comparator feeds a Schmitt-trigger. The output of the comparator is used to turn on LED 1, which is used to indicate a disturbance at the input voltage. The output of the comparator is also used to interrupt the DSP. The DSP then turns the chopper off and continues to fire the converter, thus transferring energy from the dc link to the motor. Energy for the electronic and drivers circuits are obtained from the super capacitors described previously.

After the power returns, the highest priority is the charging of the dc link capacitors. To control the charging current, the chopper is turned on for a short time and turned off again, so the current does not exceed the ratings of the devices.

During the period of the dc link capacitor charging, the firing of the converter is inhibited. To avoid the use of a second voltage sensor on the output of the chopper, an open loop charging for the capacitor is executed, assuming a worst case of the dc link capacitor being completely discharged.

In order to limit the current flowing through the chopper and the diode bridge, the firing of the motor converter is inhibited to remove an additional parallel path to the dc link capacitor. The time duration to fire is determined from a PSPICE simulation as shown in Fig. 6. Once the nominal voltage for the capacitor is obtained, the SRM converter is fired again.

III. MODELING OF THE SWITCHED RELUCTANCE MOTOR

The outward simplicity of construction and relatively easy working principles belies the complexity of the mathematical modeling for performance prediction, due to the severe saturation of the iron. The saturation is particularly severe when a narrow airgap for improved energy conversion efficiency is

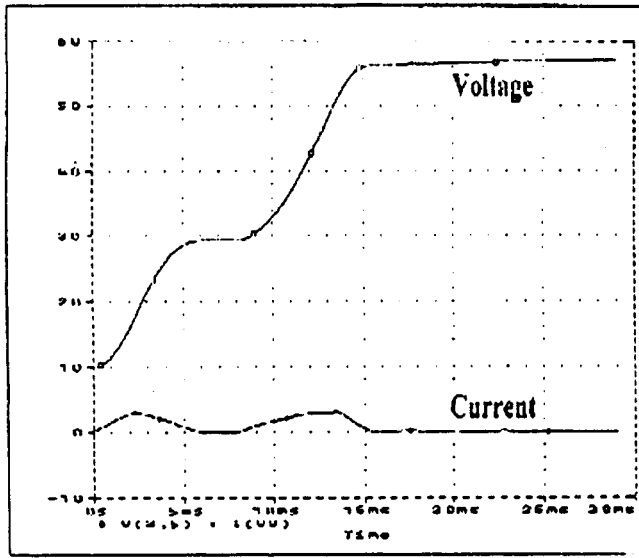


Fig. 6. Charging current and voltage waveforms using PSPICE simulation.

used. The high degree of difficulty in modeling of the SRM is due to the nonlinear electrical phase equation, represented in several different forms as follows:

$$\frac{d\psi(i, \theta)}{dt} = v - Ri(\psi, \theta) \quad (2.1)$$

$$\frac{di(\psi, \theta)}{dt} = \left(\left[\frac{d\psi}{dt} \right]^{-1} \right) \left(v - iR - \omega \frac{d\psi}{d\theta} \right) \quad (2.2)$$

$$\frac{di}{dt} = \left[\frac{1}{l} \right] \left(v - iR - i\omega \left[\frac{\delta L}{\delta \theta} \right] \right) \quad (2.3)$$

$$\frac{di}{d\theta} = \frac{1}{\omega} \left(1 + \left[\frac{\delta \psi}{\delta i} \right] \right) \left(v - iR - \left[\frac{\delta \psi}{\delta \theta} \right] \omega \right) \quad (2.4)$$

$$\frac{d\psi}{dt} = g(i - f(\psi(t))) \quad (2.5)$$

where

- Ψ_k = Flux linkage of phase k in WbT.
- v_k = Applied voltage of phase k in Volts.
- i_k = Phase current of phase k in Amps.
- R = Phase Resistance in Ohms.
- ω = Rotor speed in Rad/Sec
- T_e = Electromagnetic Torque in Nm
- T_l = Load torque in Nm
- θ = Rotor angle in mechanical Rad
- $W'(\theta, i)$ = Coenergy function
- l = Incremental inductance
- L = Slope of line from origin to instantaneous flux
- g = a function of current and flux linkage
- f = a function of flux linkage

It is obvious that the above equations have no analytical solution as the flux linkage is a nonlinear function of current and rotor angle and the equations have two unknowns, Ψ and i . The attempts to model SRMs basically differs on the variable chosen for solution and hence the requirement of different data sets.

The operation and hence the modeling of SRMs is entirely different from conventional motors. The complication in modeling the SRM is due to the nonlinear nature of the motor for the following reasons.

- 1) The iron inside the motor is highly saturated for improved energy conversion efficiency.
- 2) Dependence of motor parameters on switching strategy.
- 3) Dependence of static torque, flux linkage and inductance on both rotor position and excitation current.
- 4) Uneven distribution of flux in both rotor and stator cores.

Since the SRM characteristics are nonlinear, no constant parameter equivalent circuit is possible. The dynamics of the SRM are governed by the following electrical equations for a 4-phase SRM

$$\frac{d\psi_a}{dt} = v_a - i_a R_a \quad (2.6)$$

$$\frac{d\psi_b}{dt} = v_b - i_b R_b \quad (2.7)$$

$$\frac{d\psi_c}{dt} = v_c - i_c R_c \quad (2.8)$$

$$\frac{d\psi_d}{dt} = v_d - i_d R_d \quad (2.9)$$

and the following mechanical equations

$$\frac{d\omega}{dt} = \frac{T_e - T_l}{J} \quad (2.10)$$

$$\frac{d\theta}{dt} = \omega. \quad (2.11)$$

The static characteristic equations are

$$W'(\theta, i) = \int_0^i \psi(\theta, i) di \Big|_{\theta=\text{constant}} \quad (2.12)$$

$$T(\theta, i) = \frac{\delta W'(\theta, i)}{\delta \theta} \Big|_{i=\text{constant}} \quad (2.13)$$

IV. MODELING OF THE RECTIFIER

A. Introduction

In order to derive the rectifier model, it is necessary to consider the overlap angles of the diodes during the transfer of current conduction from one diode to another. The overlap is caused by source inductance present on the supply side, the neglect of which can cause serious errors in the calculation of the output voltage of the rectifier. The rectifier model for the switched reluctance motor drive has been derived by considering the effects of overlap as well as current and voltage harmonics. The effects of the overlap have been considered by comparing the instantaneous values of the terminal phase voltages at the input of the rectifier.

The voltage and current equations for the drive circuit have been derived using the different conduction sequences. Considering that there will be no more than three diodes in conduction at a time, a three phase bridge rectifier can have a total of 12 conduction sequences. During a single phase or three phase fault, a thirteenth nonconducting sequence may occur when the dc link current becomes discontinuous and the line currents are interrupted.

According to Fig. 7, topology "1" corresponds to a conduction sequence in which diodes $D1$ and $D2$ are conducting. On

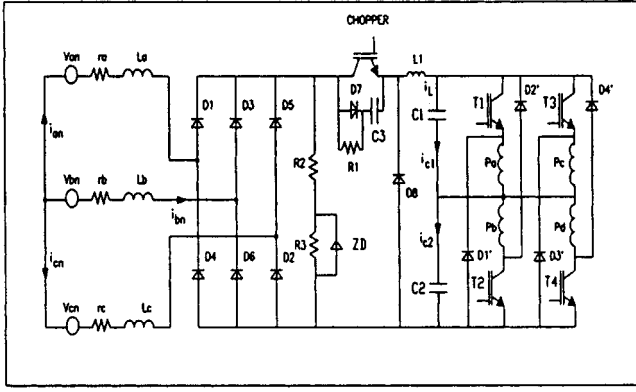


Fig. 7. Circuit diagram for the chopper controlled drive.

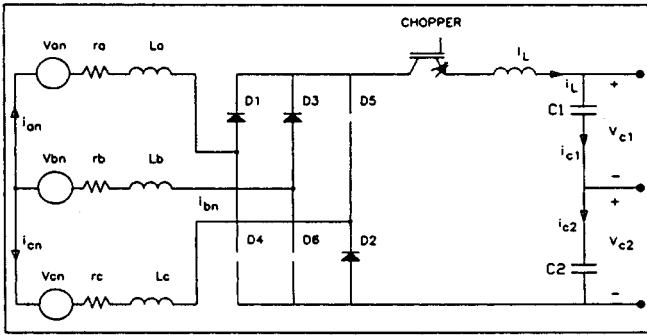


Fig. 8. Effective circuit for conduction sequence 1.

the other hand, in topology “2,” $D1$, $D2$ and $D3$ are in conduction. This sequence of conduction happens when current commutates from phase “a” to phase “b.”

The duration of the overlap depends on the source parameters and the dc link current. If we consider no more than three diodes conducting simultaneously, then the overlap angle can vary from zero to 60 degrees. Overlap angles greater than 60 degrees, and simultaneous conduction of four diodes occurs quite rarely under special circumstances and therefore not included here. After commutation is complete, diodes 2 and 3 start conducting.

Determination of Conduction Sequences—See Table II.

B. Equivalent Circuit for the Rectifier

1) *Equivalent Circuit with the Chopper Conducting:* In this section, the equivalent circuits of the rectifier for different conduction sequences are depicted in circuit diagrams. Then the mathematical model for the corresponding circuits are then written by using Kirchoff’s Voltage Law.

Conduction Sequence 1: The effective circuit for this conduction sequence is given in Fig. 8 where diodes $D1$ and $D2$ are in conduction.

The governing equations are

$$\begin{aligned} V_{an} - r_a i_{an} - L_a p i_{an} - r_l i_{an} - L_l p i_{an} \\ - V_{c1} - V_{c2} - L_c p i_{an} - r_c i_{an} - V_{cn} = 0 \end{aligned} \quad (4.1)$$

$$p i_{an} = \frac{V_{an} - V_{cn} - (r_a + r_l + r_c) i_{an} - V_{c1} - V_{c2}}{L_a + L_l + L_c} \quad (4.2)$$

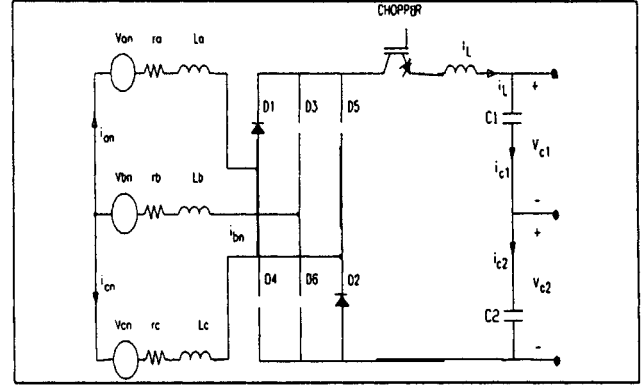


Fig. 9. Effective circuit for conduction sequence 2.

$$p V_{c1} = \frac{i_{an} - i_m}{C_1}, \quad p V_{c2} = \frac{i_{an} - i_b - i_d}{C_2} \quad (4.3)$$

$$i_{cn} = -i_{an} \quad i_{bn} = 0. \quad (4.4)$$

Conduction Sequence 2: The effective circuit for this conduction sequence is given in Fig. 9 where diodes $D1$, $D2$, and $D3$ are in conduction.

The governing equations are

$$\begin{aligned} V_{an} - r_a i_{an} - L_a p i_{an} + L_b p i_{bn} + r_b i_{bn} \\ = V_{bn} - (-L_a p i_{an} + L_b p i_{bn}) \\ = -(V_{bn} - V_{an} - r_b i_{bn} + r_a i_{an}) \end{aligned} \quad (4.5)$$

$$\begin{aligned} V_{bn} - r_b i_{bn} - L_b p i_{bn} - (r_l + r_c)(i_{an} + i_{bn}) - (L_l + L_c) \\ \cdot p(i_{an} + i_{bn}) - V_{c1} - v_{c2} \\ = V_{cn} - (L_l + L_c) p i_{bn} - (L_b + L_l + L_c) p i_{an} \\ = (V_{cn} - V_{bn} + V_{c1} + V_{c2} + (r_b + r_l + r_c) i_{bn} + (r_l + r_c) i_{an}) \end{aligned} \quad (4.6)$$

$$\begin{aligned} V_{an} - r_a i_{an} - L_a p i_{an} - (r_l + r_c)(i_{an} + i_{bn}) - (L_l + L_c) \\ \cdot p(i_{an} + i_{bn}) - V_{c1} - v_{c2} \\ = V_{cn} - (-L_l + L_c) p i_{an} - (L_a + L_l + L_c) p i_{bn} \\ = (V_{cn} - V_a + V_{c1} + V_{c2} + (r_a + r_l + r_c) i_{an} + (r_l + r_c) i_{bn}). \end{aligned} \quad (4.7)$$

Combining the above equations we obtain the following equations in Matrix form

$$\begin{aligned} \begin{vmatrix} L_a & -L_b \\ L_b + L_l + L_c & L_l + L_c \\ L_l + L_c & L_a + L_l + L_c \end{vmatrix} p \begin{vmatrix} i_{an} \\ i_{bn} \end{vmatrix} \\ = \begin{vmatrix} V_{an} - V_{bn} - r_a i_{an} + r_b i_{bn} \\ (V_{bn} - V_{cn} - V_{c1} - V_{c2} \\ -(r_b + r_l + r_c) i_{bn} - (r_l + r_c) i_{an}) \\ V_{an} - V_{cn} - V_{c1} - V_{c2} \\ -(r_a + r_l + r_c) i_{an} - (r_l + r_c) i_{bn} \end{vmatrix} \end{aligned} \quad (4.8)$$

In a similar manner, the other conduction sequences described in Table I can be derived.

2) *Equivalent Circuits with the Chopper Off:* Here, the equivalent circuits of the rectifier and corresponding equations for different conduction sequences are presented with the

TABLE I
SHOWS THE DIFFERENT CONDUCTION SEQUENCES FOR A THREE
PHASE BRIDGE RECTIFIER

Con	D	I	O	D	E	S
seq.	D1	D2	D3	D4	D5	D6
1	ON	ON	OFF	OFF	OFF	OFF
2	ON	ON	ON	OFF	OFF	OFF
3	OFF	ON	ON	OFF	OFF	OFF
4	OFF	ON	ON	ON	OFF	OFF
5	OFF	OFF	ON	ON	OFF	OFF
6	OFF	OFF	ON	ON	ON	OFF
7	OFF	OFF	OFF	ON	ON	OFF
8	OFF	OFF	OFF	ON	ON	ON
9	OFF	OFF	OFF	OFF	ON	ON
10	ON	OFF	OFF	OFF	ON	ON
11	ON	OFF	OFF	OFF	OFF	ON
12	ON	ON	OFF	OFF	OFF	ON
13	OFF	OFF	OFF	OFF	OFF	OFF

TABLE II
DESCRIBES THE CONDITIONS TO DETERMINE DIFFERENT
CONDUCTION SEQUENCES

Condition	Conduction sequences
$V_{ap} > V_{cp}$	1
$V_{ap} > V_{cp}, V_{bp} > V_{ap}, I_{an} > 0, I_{cn} < 0$	2
$V_{bp} > V_{cp}$	3
$V_{bp} > V_{cp}, V_{ap} > V_{cp}, I_{bn} > 0, I_{cn} < 0$	4
$V_{bp} > V_{ap}$	5
$V_{bp} > V_{ap}, V_{cp} > V_{bp}, I_{bn} > 0, I_{an} < 0$	6
$V_{cp} > V_{ap}$	7
$V_{cp} > V_{ap}, V_{bp} > V_{ap}, I_{cn} > 0, I_{an} < 0$	8
$V_{cp} > V_{bp}$	9
$V_{cp} > V_{bp}, V_{ap} > V_{cp}, I_{cn} > 0, I_{bn} < 0$	10
$V_{ap} > V_{bp}$	11
$V_{ap} > V_{bp}, V_{bp} > V_{cp}, I_{an} > 0, I_{bn} < 0$	12

chopper off. The equations are written by using Kirchoff's Voltage Law.

Conduction Sequences 1, 3, 5, 7, 9, and 11: The effective circuit for these conduction sequences are the same and is given

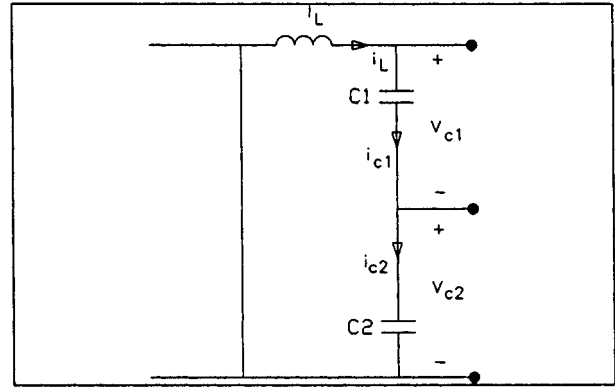


Fig. 10. Effective circuit for conduction sequences 1, 3, 5, 7, 9 and 11.

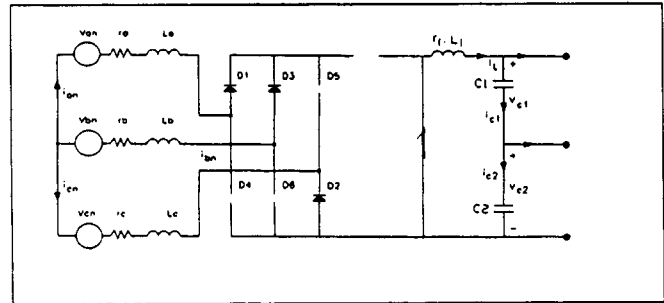


Fig. 11. Effective circuit for conduction sequence 2.

in Fig. 10, where diodes $D1$ and $D2$, $D2$ and $D3$, $D3$ and $D4$, $D4$ and $D5$, $D5$ and $D6$, or $D6$ and $D1$ are in conduction.

The governing equations are

$$C_1 \frac{dv_{c1}}{dt} = i_L - i_{c1} \quad (4.12)$$

$$C_2 \frac{dv_{c2}}{dt} = i_L - i_{c2} \quad (4.13)$$

$$L \frac{di_L}{dt} = -v_{c1} - v_{c2} - r_L i_L. \quad (4.14)$$

The effective circuit for this conduction sequence is given in Fig. 11, where diodes $D1$, $D2$, and $D3$ are in conduction.

The governing equations are

$$(L_a + L_b) \frac{di_{an}}{dt} = v_{an} - v_{bn} - (r_a + r_b) i_{an} \quad (4.15)$$

$$i_{bn} = -i_{an} \quad i_{cn} = 0 \quad (4.16)$$

$$C_1 \frac{dv_{c1}}{dt} = i_L - i_{c1} \quad (4.17)$$

$$C_2 \frac{dv_{c2}}{dt} = i_L - i_{c2} \quad (4.18)$$

$$L \frac{di_L}{dt} = -v_{c1} - v_{c2} - r_L i_L. \quad (4.19)$$

In a similar manner, the equations for the other even numbered conduction sequences can be written.

V. RIDE-THROUGH CAPABILITY RESULTS

To start the machine the capacitors $C1$ and $C2$ shown in Fig. 7 must be charged. To control the charging current, the capacitors

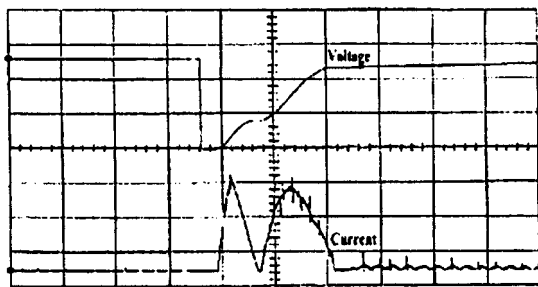


Fig. 12. Charging voltage and current for the D.C. link capacitors. 20 V/div (top), 1 A/div (lower), 10 ms/div.

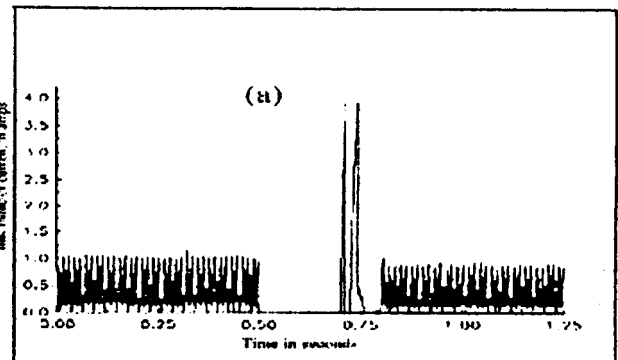
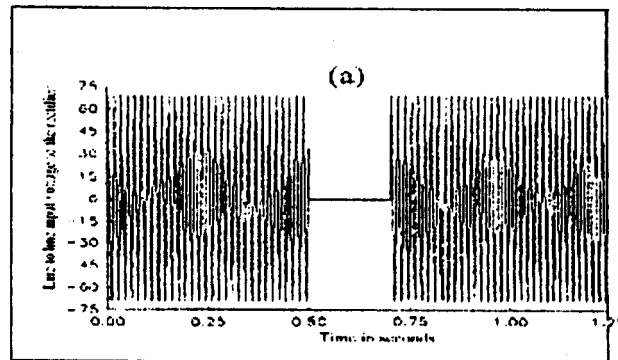
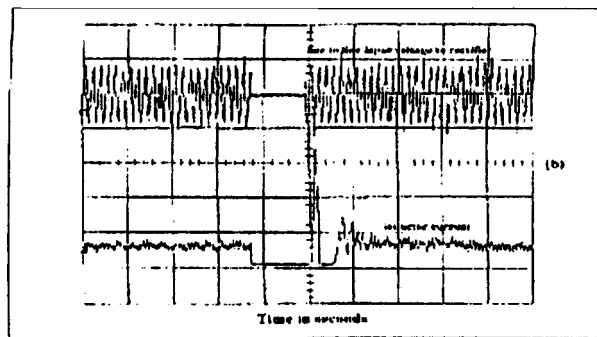


Fig. 14. Line to line input voltage of bridge rectifier and inductor current. 20 V/div, 1 A/div, 100 ms/div. (a) Predicted, (b) actual.

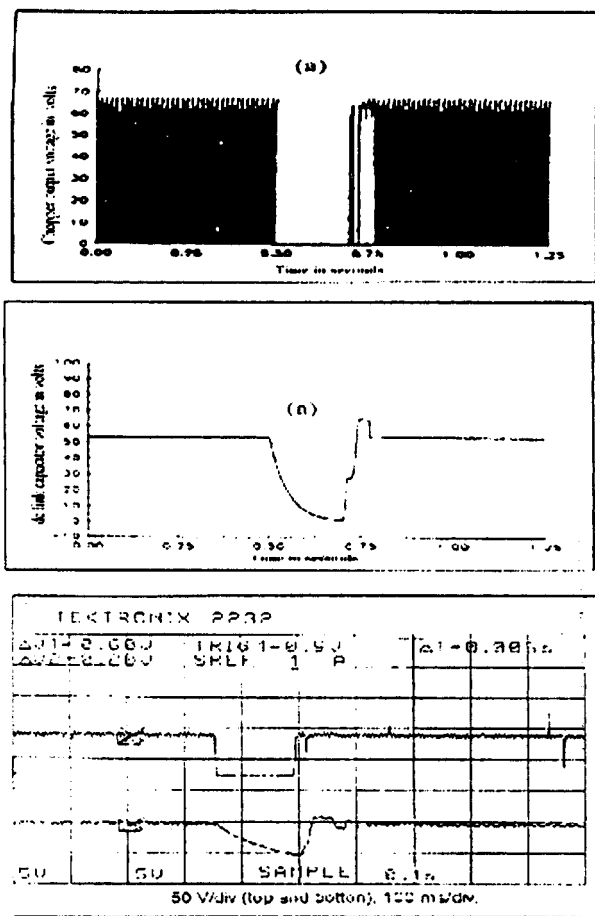


Fig. 13. Rectifier output and dc link capacitor voltages. 50 V/div (top and bottom), 100 ms/div. (a) Predicted, (b) actual.

are charged in two steps. Fig. 12 shows the measured results of the capacitors being charged with the current being controlled by turning the chopper ON and OFF in two steps. This measured result is in agreement with the predicted results from PSPICE shown in Fig. 6.

Using the super capacitors to supply energy to the logic circuit and to the driver circuits, the ability of the motor drive to ride through a short duration outage is now shown. A circuit breaker supplying the output to the rectifier was opened for 160 ms (10 cycles approximately).

Figs. 13–18 show the predicted results from computer simulation as well as actual experimental results. The experimental

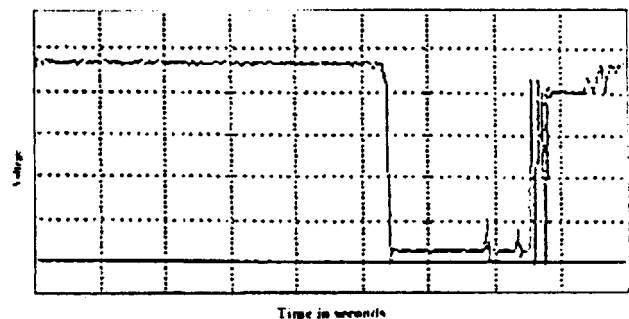


Fig. 15. Actual duty cycle chopper control. 1 V/div, 100 ms/div.

results closely follow the results predicted by computer simulation. Fig. 13 shows the output voltage of the bridge rectifier on the top trace and the dc link capacitor voltage on the bottom. During the interruption, the rectifier output falls

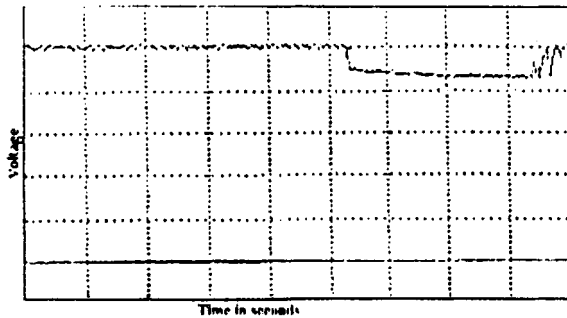


Fig. 16. Actual chopper voltage of the super capacitor 1 V/div, 100 ms/div.

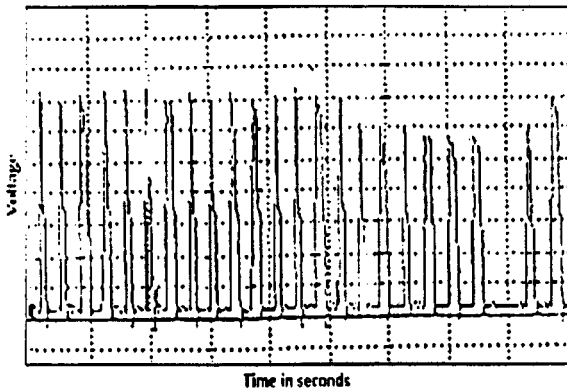


Fig. 17. Actual gate drive for phase A 5 V/div, 100 ms/div.

to zero while the voltage of the capacitors decay toward zero as it supplies power to the motor. Once the power returns, the output voltage of the rectifier jumps to its normal value and the dc link capacitors are charged assuming a zero initial voltage. Thus the charging in the two steps can be seen in the bottom trace, which is similar to that shown in Fig. 12. The capacitor is charged to its nominal value. Because the phases are off when the power comes back, no current flows through the chopper after the dc link capacitor is charged. Thus the output and input voltages of the chopper are the same. Once the dc link capacitor is fully charged, the phases are turned on, and the output voltage of the chopper reduces to a level selected by the control signal.

Fig. 14 shows the line to line voltage of the input diode bridge rectifier on the top trace, and the current of the inductor $L1$ on the bottom. During normal operation, the current of the inductor is the chopper current when the chopper is on and the freewheeling current of the diode $D5$ when the chopper is off. When the power goes off, the inductor current reaches zero rapidly. When the power comes back, two peaks are shown in Fig. 14. This represents the charging current of the dc link capacitors.

Fig. 15 shows the chopper control signal, where the voltage is proportional to the chopper on-time. Before the fault, the magnitude of the signal is proportional to the speed. When the interruption is detected the chopper is turned off, but the phases are still fired as shown in Fig. 17, which shows the gate drive signal. The drop in voltage in the gate drive signal is due to the loss in mains power but with the super capacitors still supplying

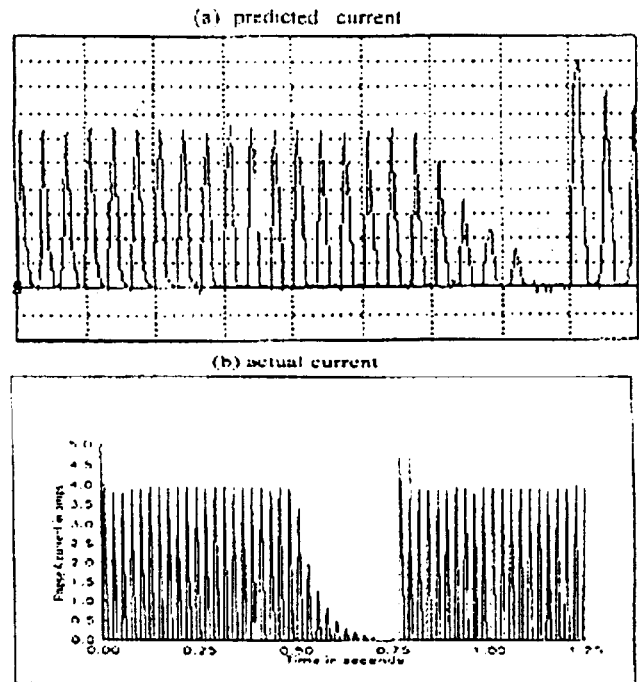


Fig. 18. Phase A current 1 A/div, 100 ms/div. (a) Predicted, (b) actual.

power to the gate drive. When the power comes back on, the firing of the phases is inhibited and the chopper turned on in 2 steps as shown in Fig. 14 to charge the capacitors. During the period of loss in power, the super capacitors also supply the logic circuitry with power as shown in Fig. 16. The gate drive signals for phase A are shown in Fig. 17. During the fault, there is a reduction in the driver voltage but it is still operating properly with the help of the supercapacitors. There is a short duration when phase A is turned off to allow charging of the dc link capacitors. The phase A current is shown in Fig. 18. During normal operation the phase A current is proportional to the load of the motor. During the fault, the phase A current gradually reduces as the dc link capacitors discharge. When firing begins again after the dc link capacitors are charged up, a larger current is drawn to accelerate the motor back up to the commanded speed.

VI. CONCLUSION

In this paper, a chopper controlled SRM drive is used to improve the ride-through capability during short-term outages. A ride through capability of around 30 cycles is provided to the logic circuitry using supercapacitors. Upon reapplication of the power, the logic circuitry is able to reaccelerate the motor, without having to bring the drive to a standstill. The use of current transducers in the dc link to control the inrush current is avoided by implementing a timed charging of the dc link capacitors. The speed response of the drive will depend on the inertia and load torque and the acceptability of the speed response will depend on the application. Predicted results from computer simulations and detailed practical measurements have been presented to demonstrate the ability of the drive to ride through power discontinuities.

APPENDIX A
 FLUX-LINKAGE VS CURRENT CURVE PHASE RESISTANCE =
 0.77 ohms

Flux current curve of the switched reluctance motor

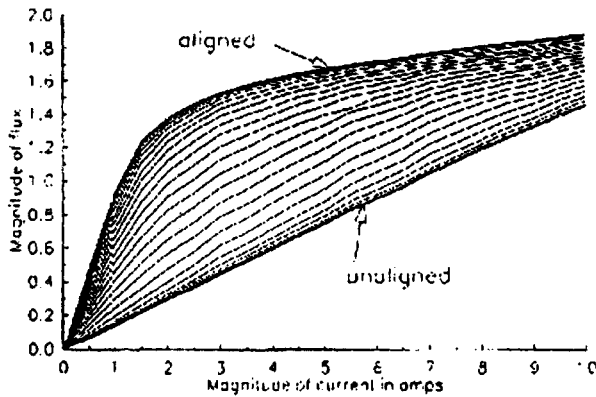


Fig. 19. Flux current curve of the switched reluctance motor.

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