

```
library IEEE;
use IEEE.std_logic_1164.all;
```

```
entity v74x153 is
```

```
  port (
    A: in STD_LOGIC;
    B: in STD_LOGIC;
    G_L: in STD_LOGIC_VECTOR (1 to 2);
    C0: in STD_LOGIC_VECTOR (1 to 2);
    C1: in STD_LOGIC_VECTOR (1 to 2);
    C2: in STD_LOGIC_VECTOR (1 to 2);
    C3: in STD_LOGIC_VECTOR (1 to 2);
    Y: out STD_LOGIC_VECTOR (1 to 2)
```

```
  );
```

```
end v74x153;
```

```
architecture v74x153_arch of v74x153 is
```

```
  signal S:STD_LOGIC_VECTOR (0 to 3);
```

```
begin
```

```
S <= G_L(1)&G_L(2)&B&A;
```

```
with S select
```

```
  Y <= C0 when "0000",
    C1 when "0001",
    C2 when "0010",
    C3 when "0011",
    C0(1)&'0' when "0100",
    C1(1)&'0' when "0101",
    C2(1)&'0' when "0110",
    C3(1)&'0' when "0111",
    '0'&C0(2) when "1000",
    '0'&C1(2) when "1001",
    '0'&C2(2) when "1010",
    '0'&C3(2) when "1011",
    "00" when others;
```

```
end v74x153_arch;
```