

## EE 365 Take Home Exam

1. (5 points) (a) Let  $X=0011\ 1110\ 1010$  and  $Y=1011\ 0011\ 1010$ . If these two 12 bit numbers were applied as inputs to the comparator circuit as shown in Fig. 5-82 (page 424). Simulate the circuit using **demolib** library in your Xilinx's Foundation software. Evaluate the outputs (logical 1 or 0) at pins 2, 3, 4 (ALTBIN, AEQBIN and AGTBIN) and 5, 6 & 7 (AGTBOUT, AEQBOUT & ALTBOU, respectively) of the three 74LS85 MSI chips. Briefly explain your answer and present it in a tabular form. (b) Derive a logic expression for the arithmetic comparison ( $A < B$ ). Hint: look at the expression for ( $A > B$ ) on page 424.
  
2. (5 points) This problem is based on Exercise #5.91 on page 466. (Hint: you will need 74x153 & 74x157 MSI chips for this). Do not use more than 3 chips. The overall project will be done in the schematic mode in Xilinx's Foundation software. However, the "blocks" that represent the above-mentioned chips must be described using VHDL in the form of a macro. Describe the **74x153** in the behavior design elements and the **74x157** in the dataflow elements of the VHDL program.
  
3. (5 points) Analyze the following state machine. Write excitation equations, transition table, and the state/output table. Draw the State Diagram. (Use State names A, B, C, D for  $Q_2Q_1 = 00, 01, 10, 11$ , respectively.) Complete the timing diagram as shown below without using the Xilinx software. Assume that at  $t=0$ ,  $Q_2Q_1=00$ .

