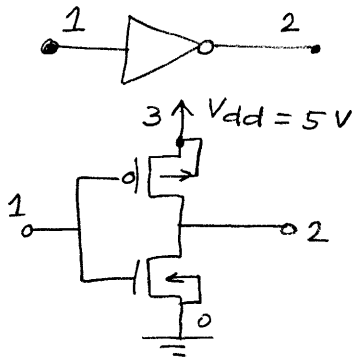
* Delays in a CMOS transmission gate 2-1_MUX circuit

```
.model ndev nmos(level=2,vto=1.0,tox=150e-10,kp=40e-6,gamma=0.0)
.model pdev pmos(level=2,vto=-1.0,tox=150e-10,kp=20e-6,gamma=0.0)
```

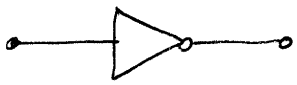
* This is a subcircuit of an inverter (W_n=3um, W_p=6um and L=1um)

```
.subckt inv 1 2 ; input , output
mn1 2 1 0 0 ndev w=3um l=1um
mp1 2 1 3 3 pdev w=6um l=1um
c_lumped 2 0 0.01p
Vdd 3 0 5.0
.ends
```



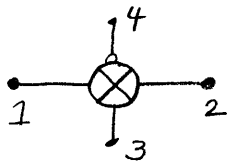
* This is a subcircuit of another inverter

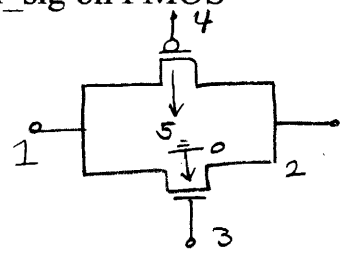
```
.subckt invw1 1 2 ; input , output
mn1 2 1 0 0 ndev w=3um  l=1um
mp1 2 1 3 3 pdev w=6um l=1um
c_lumped 2 0 0.01p
Vdd 3 0 5.0
.ends invw1
```



* This is a subcircuit of a Transmission Gate

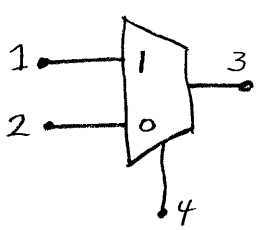
```
.subckt trg 1 2 3 4 ;input, output, contrl_sig on NMOS, contrl_sig on PMOS
mn 1 3 2 0 ndev w=3um l=1um
mp 1 4 2 5 pdev w=6um l=1um
Vdd 5 0 5.0
.ends trg
```

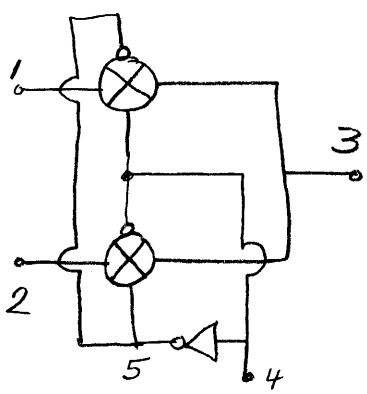




*This is for a 2-1 MUX

```
.subckt mux2to1 1 2 3 4 ; input1, input2, output, address
xtrg1 1 3 4 5 trg
xinv 4 5 inv
xtrg2 2 3 5 4 trg
.ends
```





* Main Input file

```
xmux1 1 2 8 10 mux2to1
xinv1 11 1 invw1
xinv2 22 2 invw1
c_load    8 0 0.5pf
r_shunt  8 0 100MEG

vin1     11  0 pulse(0 5 0ns 1ns 1ns 3ns 8ns)
vin2     22  0 pulse(5 0 0ns 1ns 1ns 7ns 16ns)
v_add  10 0 pulse(0 5 25ns 1ns 1ns 24ns 50ns)

.option itl5=0
.tran .1ns 60ns 0.0ns 0.1ns
.probe
.end
```