library IEEE;
use IEEE.std_logic_1164.all;
-- Uses Behavioral Design elements

entity v74x157 is
  port ( 
    G_L: in STD_LOGIC;
    S: in STD_LOGIC;
    A: in STD_LOGIC_VECTOR (1 to 4);
    B: in STD_LOGIC_VECTOR (1 to 4);
    Y: out STD_LOGIC_VECTOR (1 to 4)
  );
end v74x157;

architecture v74x157_arch of v74x157 is
begin
  S1 <= G_L & S;

  process(S1,A,B)
  begin
    case S1 is
      when "00" => Y <= A;
      when "01" => Y <= B;
      when others => Y <= "0000";
    end case;
  end process;
end v74x157_arch;