Chapter 3

24. (a) $P = \left( \frac{I_{ccH} + I_{ccL}}{2} \right) \frac{V_{cc}}{2} = \left( \frac{1.6\text{mA} + 4.4\text{mA}}{2} \right) \times (5.5) = 16.5\text{ mV}$

(b) $V_{oh\ min} = 2.7\text{V}$

(c) $t_{PLH} = t_{PHL} = 15\text{ns}$

(d) $V_{OL} = 0.4\text{V (}@I_{OL} = 4.0\text{mA}@I_{OL} = 8.0\text{mA})$
   $V_{OL} = 0.5\text{V @ }I_{OL} = 8.0\text{mA}$

(e) $t_{PLH} = t_{PHL} = 110\text{ns (}@V_{cc} = 2\text{V @ }T = 125\text{°C}@V_{cc} = 3\text{V @ }T = 125\text{°C})$
   $t_{PLH} = 55\text{ns (}@V_{cc} = 3\text{V @ }T = 125\text{°C}@V_{cc} = 4.5\text{V @ }T = 125\text{°C})$

26. Gate A can be operated at a higher frequency because it has a shorter propagation delay than that of gate B.

46. Board Position

Component in Chamber

Activate insertion tool

48. Enable

\[ \text{RESET} \]
Chapter 14

1. \( \text{Noise margin}_H = V_{OH}^{(min)}_1 - V_{IH}^{(min)}_2 = 2.2 - 2.5 = -0.3 \leq 0 \)

   No, they are not compatible.

2. \( \text{Noise margin}_L = V_{IL}^{(max)}_2 - V_{OL}^{(max)}_1 = 0.75 - 0.45 = 0.3 \geq 0 \)

   Yes, they are compatible.

4. \( \text{Noise margin}_H = V_{OH}^{(min)}_1 - V_{IH}^{(min)}_2 = 2.4 - 2.25 = 0.15 \text{V} \)
   \( \text{Noise margin}_L = V_{IL}^{(max)}_2 - V_{OL}^{(max)}_1 = 0.65 - 0.4 = 0.25 \text{V} \)

   Maximum amplitudes of noise spikes equal the noise margins of 0.15 \& 0.25 for high \& low, respectively.

6. \( P_D (\text{low}) = (5 \text{V})(2\text{mA}) = 10 \text{mW} \)
   \( P_D (\text{high}) = (5 \text{V})(3.5\text{mA}) = 17.5 \text{mW} \)
   \( P_D (\text{avg}) = (10 + 17.5)/2 = 13.75 \text{mW} \)

9. \( \text{Average prop delay} = \frac{1\text{ns} + 1.2\text{ns}}{2} = 1.1\text{ns} \)
   \( \text{Speed-power product} = (1.1\text{ns})(15\text{mW}) = 16.5\text{pJ} \)
\[ \text{Gate B} \]
\[
\text{Average prop delay} = \frac{5 + 4}{2} = 4.5 \text{ ns}
\]
\[
\text{Speed-power product} = (4.5 \text{ ns})(8 \text{ mW}) = 36 \text{ pJ}
\]

\[ \text{Gate C} \]
\[
\text{Average prop delay} = \frac{10 \text{ ns} + 10 \text{ ns}}{2} = 10 \text{ ns}
\]
\[
\text{Speed-power product} = (10 \text{ ns})(0.5 \text{ mW}) = 5 \text{ pJ}
\]

11. \( S_2 \) is overloaded because it has 12 loads.

16. (a) ON: high voltage on base forward-biases the base-emitter junction

(b) OFF: insufficient voltage. Need 0.6 - 0.7V

(c) OFF: Base voltage lower than emitter

(d) OFF: Base & emitter at same voltage

18. Connect 1k resistor pull-up to unused input of NAND gates & connect the unused input of NOR gate to ground.

Connect the pull-up resistor to the open collector of the output.
20. (a) The driving gate (G1) output is high. It is sourcing 3 unit loads.
   \[ I_T = 3 \times 40\mu A = 120\mu A \]

(b) The driving gate output is low. It is sinking current from 2 unit loads.
   \[ I_T = 2 \times 1.6\, mA = 3.2\, mA \]

(c) G1 output is high.
   \[ I_T(G1) = 6 \times 40\mu A = 240\mu A \) (Sourcing)
   G2 output is low.
   \[ I_T(G2) = 2 \times 1.6\, mA = 3.2\, mA \) (Sinking)
   G3 output is high.
   \[ I_T(G3) = 2 \times 40\mu A = 80\mu A \]