Solution to HW #4

12. \( A \quad D \quad B \quad X \)

\( AND \quad B \)

\( x = 1 \) when both \( A \) and \( B \) are \( 1 \)

13. \( A \quad B \quad C \quad D \quad X \)

\( NAND \quad B \quad C \quad D \quad X \)

\( x = 0 \) when \( A, B, C, D \) are all \( 1 \)

16. \( A \quad B \quad C \quad X \)

\( NOR \quad B \quad C \quad X \)

Output \( x = 1 \) when \( A, B, C \) are all \( 0 \)

20. \( A \quad B \quad X \)

\( A \quad D \quad X \)

Note: From the truth table

- if \( B = 1 \), \( x = \overline{A} \) (Inverted)
- if \( B = 0 \), \( x = A \) (i.e., \( x \) is same)
See problem #20:
X in this case will be inverted.
with respect to the solution
shown in #20.

\[ x_1 = (\overline{A} \cdot B) \]
\[ x_2 = (\overline{A} \cdot B) \]
\[ x_3 = (A \cdot B) \]

```
entity AND3 is
port (A, B, C: in bit; 
    X: out bit);
end entity AND3;
architecture AND3.arch of AND3 is
begin
    X <= (A and B) and C;
end architecture AND3.arch;
```

We can also write: \( X \leq A \text{ and } B \text{ and } C \).

NAND gate

3-input OR gate