Solution to HW #1

3(a) \[ 11010001 \]

5(c) \[ 3.2\mu s - 0.5\mu s = 2.7\mu s \]

6. \[ 4\mu s \]

7. \[ f = \frac{1}{T} = \frac{1}{4\mu s} = \frac{1}{4}\text{kHz} \]
\[ = 250\text{Hz} \]

15(c)

[Diagram of a multiplexer]

22. SPLD: Simple Programmable Logic Devices
CPLD: Complex Programmable Logic Devices
HDL: Hardware Description Language
FPGA: Field Programmable Gate Array
GAL: Generic Array Logic

25. 3 levels: ① High-level ② Assembly ③ Machine

28. A minimum VHDL code consists of
⑴ an entity ⑵ an architecture

29. Structural: A logic function is described using gates and their interconnections.

Data flow: A logic function is described using Boolean expressions (or flow of data)

Behavioral: A logic function is described of what happens on outputs in response to inputs of the system

31. Keywords: entity, architecture, port, and