1. (2.5 points) The waveforms below are applied to a gated D-latch and a positive edge-triggered D-Flip-flop. Determine the Q outputs waveform for the gated latch Q (latch) and the D- positive edge-triggered D-flip-flop Q (FF).
2. (2.5 points) The waveforms below are applied to a positive edge-triggered J-K flip-flop. Determine the Q output starting in the SET state.

3. (2.5 Points) Draw the timing diagram for the Q output of an R-S latch.

4. (2.5 Points) Answer the following question briefly.

(a) What is the major advantage of the J-K flip-flop over the S-R flip-flop?
   J-K FF has no invalid state. Instead it has a toggle state. S-R FF does not have a toggle state.

(b) What is the major difference between half-adders and full-adders?
   Full adders add two 1-bit numbers and a carry-in. Half adders do not have a carry-in input.
5. (5 Points) The following two VHDL codes have several syntax errors. Find
the errors and correct them.

(a)

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity NOT is
  port (A : in std_logic;
        X: out std_logic);
end NOT;

architecture dataflow of NOT is
begin
  X <= not A;
end dataflow;
```

(b)

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity AND2 is
  port (A, B: in std_logic;
        X: out std_logic);
end AND2;

architecture beh of AND2 is
begin

  process (A, B)
  begin
    Variable V1;
    V1 := A and B;
    X <= V1;
  end process;
```

- In (a), the reserved word `NOT` is misspelled as `N0T`.
- In (b), the process block is missing a semi-colon at the end.
- In (b), the reserved word `and` is misspelled as `ad`.
- In (b), the assignment `X <= V1` is missing a semi-colon.
6. (5 Points) (a) A logic circuit has two 4-bit words $X = X_2X_1X_0$ and $Y = Y_3Y_2Y_1Y_0$ as inputs and two 1 bit outputs $Y$ and $Z$. Design the logic circuit such that $Y = 0$ when one of the following conditions is false and $Z = 1$ when only one of the three are true.

- $X_1$ is not equal to $Y_3 \cdot Y_1$
- $X_2$ is equal to $Y_3 \oplus Y_0$
- $X_0$ is equal to $(X_2 + Y_2)'$

\[
\begin{array}{c}
Y_3 \\
Y_1 \\
X_1 \\
X_2 \\
Y_0 \\
Y_3 \\
X_0 \\
X_2 \\
Y_2
\end{array}
\]

\[
\begin{array}{c|c|c|c}
A & B & C & Y \\
0 & 0 & 0 & 0 \\
0 & 0 & 1 & 1 \\
0 & 1 & 0 & 0 \\
0 & 1 & 1 & 1 \\
1 & 0 & 0 & 1 \\
1 & 0 & 1 & 0 \\
1 & 1 & 0 & 0 \\
1 & 1 & 1 & 1 \\
\end{array}
\]

\[
Z = (\overline{A} \cdot \overline{B} \cdot C) + (\overline{A} \cdot B \cdot \overline{C}) + (A \cdot \overline{B} \cdot \overline{C})
\]
7. (5 points) Using only 4:1 MUXs (4-input data selectors) design the Boolean function \( F(C, B, A) = \sum m(1, 2, 4, 7) \).

8. (Bonus 5 points) The BCD/DEC decoder shown in Figure 6-21 is examined with a logic analyzer and the results are shown in the waveforms accompanying Figure 6-21. What, if anything, is wrong with the circuit?

   a. The "2" output is shorted internally to High ('1').
   b. The A1 input is internally not connected.
   c. The A1 input node is internally stuck LOW ('0').
   d. Nothing is wrong with the circuit.

   ![Waveforms](image)